I-Cube IQ Family Data Sheet

Features

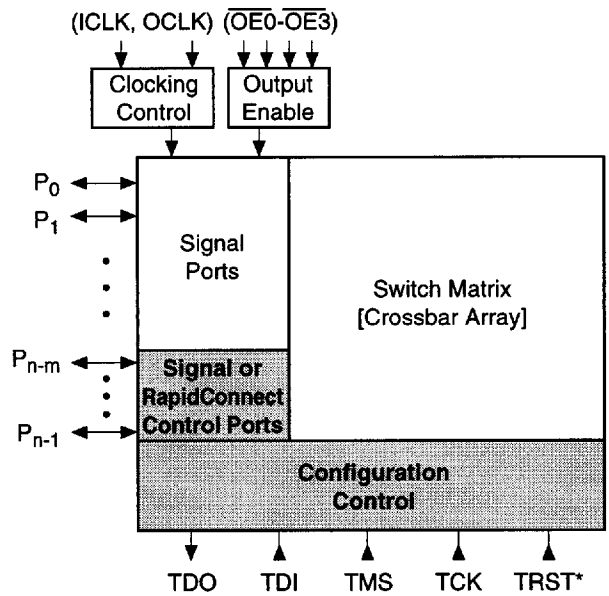
- Eight devices ranging from 32 to 320 I/O Ports
- SRAM-based Programming for In-system Reconfigurability
- Switch Matrix Architecture
  - Non-blocking
  - Predictable & Uniform Delays
  - One-to-One & One-to-Many Connections
  - Incremental Connection Changes
- Programmable I/O Ports
  - Individually Programmable as Input, Output or Bidirectional
  - Programmable TTL/CMOS Output
- Clocked and Flow-through Dataflow Modes
  - Pin-to-Pin Delay as low as 5 ns in Flow-through Mode
  - Up to 150 MHz Clock Frequency
- RapidConnect™ Interface for Switching of Connections in as fast as 20 ns
- JTAG for Boundary Scan Testing and Configuration

Description

The IQ devices are designed for use in switching and interconnect applications. In switching applications, these devices are used to dynamically switch one or more signals. When used in interconnect applications, the IQ devices allow re-routing of signals on a board or backplane.

At the heart of these devices is a non-blocking Switch Matrix, allowing total flexibility in routing signals. Every signal in the Switch Matrix can be connected to one or more other signals. The I/O Ports, connected to the Switch Matrix lines, are individually programmable as input, output or bidirectional. The IQ devices support either flow-through or clocked signal flow. The delays through the devices are identical and predictable.

The Switch Matrix connections are programmed and the I/O Port attributes are configured by storing data in the internal SRAM cells. The IQ devices use a JTAG-based serial mode for configuration. For dynamic switching, the RapidConnect interface allows fast connection changes.



	Device							
	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
n	320	240	160	128	96	64	48	32
m	24	24	20	18	18	16	15	13

n = total number of usable I/O pins
m = I/O pins used for RapidConnect

Figure 1: IQ Family Functional Block Diagram

Table of Contents

IQ Family Summary

Device	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
Number of Usable I/O	320	240	160	128	96	64	48	32
Switch Matrix Size	320	240	160	128	96	64	48	32
Pin-to-Pin Delay (ns)	12.5	12.5	10	10	6	6	5	5
NRZ Data Rate (Mbs)	133	133	160	160	200	200	250	250
Clock Frequency (MHz)	80	80	100	100	125	125	150	150
I/O Current Drive (mA)	16	16	16	16	12	12	12	12
Process (µm)	0.8	0.8	0.8	0.8	0.6	0.6	0.6	0.6
Core Voltage (V)	5	5	5	5	5	5	5	5
I/O Voltage (V)	5(1)	5(1)	5(1)	5(1)	3/5(2)	3/5(2)	3/5(2)	3/5(2)
Package(s) J=PLCC, MQ=MQUAD, PB=PBGA, PP=PPGA, PQ=PQFP, TQ=TQFP	416PB 391PP	304MQ	208MQ 208PQ	184MQ 184PQ	144MQ 144PQ 144TQ	100MQ 100PQ 100TQ 84J	80PQ 80TQ 68J	52PQ 52TQ 52J

(1) Device has common supply voltage for core and I/O buffers
(2) Device has separate supply voltages for core and I/O buffers

Table 1: The IQ Family

Architecture

The IQ devices are designed using both 0.6 and 0.8 µm CMOS technology and are configured by storing appropriate data into the internal SRAM cells and registers. The main functional blocks of the device are the Switch Matrix (Crossbar Array), I/O Ports, and Configuration Controller (see Figure 1).

External signals enter and exit each device through its I/O Ports. The Switch Matrix is used to internally connect these I/O Ports to one another.

The JTAG-based Configuration Controller decodes the incoming configuration bit stream and stores the data into the Switch Matrix SRAM cells and I/O Port configuration registers. Additionally, by enabling the RapidConnect mode, the SRAM cells can be accessed directly, allowing incremental changes (make or break) to the Switch Matrix connections in a single cycle.

Switch Matrix

Figure 2 shows a small section of the Switch Matrix.

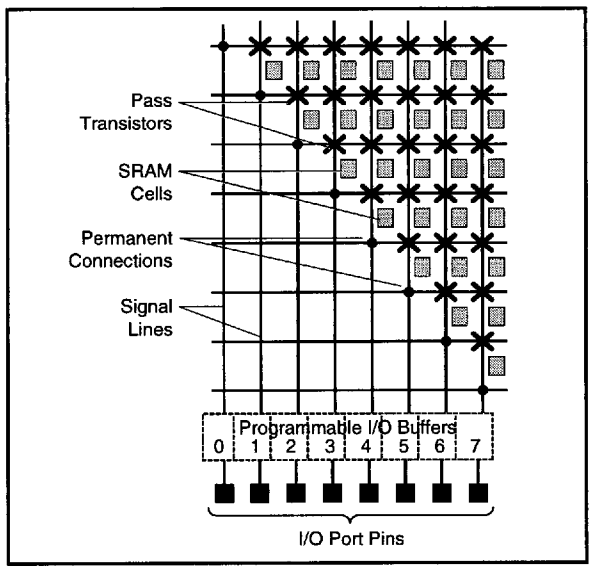


Figure 2: Switch Matrix (Crossbar Array) Structure

The Switch Matrix consists of a number of signal lines, one per I/O Port, and an array of pass transistor switches, each programmable with an SRAM cell. Each switch, when programmed to be in the ON state, connects a unique pair of signal lines in the Switch Matrix. The external signals are connected to the Switch Matrix signal lines through I/O Ports.

A connection between two I/O Ports is made by turning ON the transistor switch at the intersection of the corresponding signal lines. The Switch Matrix is globally connected, and therefore a connection can always be made between any two I/O Ports. Moreover, only one transistor switch needs to be turned ON in order to make a connection between two I/O Ports. This arrangement provides a fully non-blocking architecture offering 100% utilization, guaranteed connections, and uniform and predictable delays.

This Switch Matrix architecture supports connecting more than two I/O Ports together for multicasting/broadcasting operation. A new connection can be made or an existing connection can be broken without affecting other connections, allowing incremental reconfiguration of the Switch Matrix.

The contents of the SRAM cells controlling the pass transistor switches are unchanged when the device is reset. The SRAM cells must be explicitly cleared during initialization to eliminate any residual connections.

Programmable I/O Ports

The I/O Port structure is shown in Figure 3.

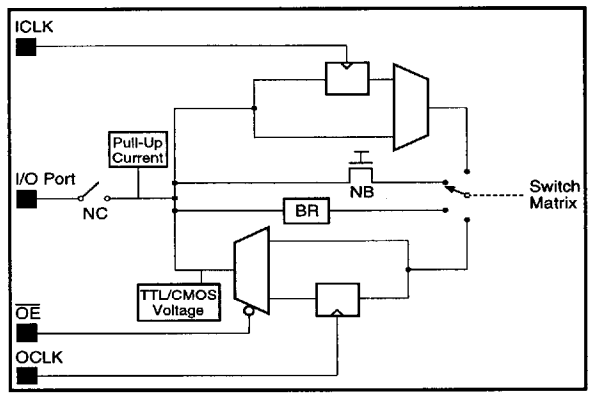


Figure 3: Programmable I/O Buffer

The attributes of each I/O Port are individually

programmable. The attributes include its I/O function, output voltage level and pull-up current. Each I/O Port is buffered to provide high input impedance, low input capacitance, low output impedance and high current drive.

The IQ devices, with the exception of IQ48 and IQ32B, have four Output Enable signals, each controlling an equal number of I/O Ports; 80 each in the case of IQ320, 60 each for IQ240B and so on. The IQ48 and IQ32B have a single Output Enable signal that controls all I/O Ports. All IQ devices have two global clock signals, ICLK and OCLK.

I/O/B Functions

Figure 4 shows the various I/O Port functions that can be programmed and are described below.

Input Modes

Input (IN) - The external signal at the I/O Port pin is connected to the corresponding Switch Matrix line through a buffer.

Registered Input (RI) - The external signal at the I/O Port pin is connected to the input of a flip-flop and the output of the flip-flop is connected to the corresponding Switch Matrix line. The clock input of the flip-flop is driven by the external clock signal, ICLK. The state of the flip-flop is not affected by device reset.

When an I/O Port is configured as an Input (IN) or Registered Input (RI), V_{IH} and V_{IL} are at TTL levels.

Output Modes

Output (OP)† - The corresponding Switch Matrix line is connected to the I/O Port pin through a buffer.

Registered Output (RO)† - The corresponding Switch Matrix line is connected to the input of a flip-flop, and the output of the flip-flop is connected to the I/O Port pin. The clock input of the flip-flop is driven by the external clock signal, OCLK. The state of the flip-flop is not affected by device reset.

Bidirectional Mode

Bus Repeater (BR)† - In the Bus Repeater mode, the I/O Port and the corresponding Switch Matrix line behave as if they were connected by a wire (with a non-zero propagation delay), allowing bidirectional signal flow. The Bus Repeater (patented by I-Cube) incorporates a self-sensing circuit to determine signal direction.

When multiple I/O Ports configured as Bus Repeater are connected together through the Switch Matrix to form a single internal node, a signal appearing at any one of the I/O Ports is repeated to the remaining I/O Ports that are a part of that node.

The Bus Repeater mode requires an external or internal (see the section on "Programmable Pull-up Current") pull-up current source to operate properly. For more details, refer to the Technical Note: "The Bus Repeater Mode" in the "Programmable Switching and Interconnect Devices - Applications Handbook".

Other Modes

Pin Side Force 0 (F0) † - The I/O Port pin is forced low (logic 0) by the internal buffer, regardless of the signal on the corresponding Switch Matrix line.

Pin Side Force 1 (F1)† - The I/O Port pin is forced high (logic 1) by the internal buffer, regardless of the signal on the corresponding Switch Matrix line.

Array Side Force 0 (A0) - The Switch Matrix line is forced low (logic 0), regardless of the signal on the corresponding I/O Port.

Array Side Force 1 (A1) - The Switch Matrix line is forced high (logic 1), regardless of the signal on the corresponding I/O Port.

Non-Buffer (NB) - The I/O buffer is bypassed and the I/O Port pin is connected to the corresponding Switch Matrix line through a pass transistor. This mode can be used to pass analog signals if certain conditions are met. Contact I-Cube for more details.

No Connect (NC) - The I/O Port pin is isolated from the Switch Matrix line.

Upon reset all I/O Ports are automatically configured as No Connect (NC).

† In these modes, the Output Enable signals control the active and Hi-Z state. The buffers are driving the pin when the corresponding Output Enable signal (see Table 7) is low, and Hi-Z when it is high.

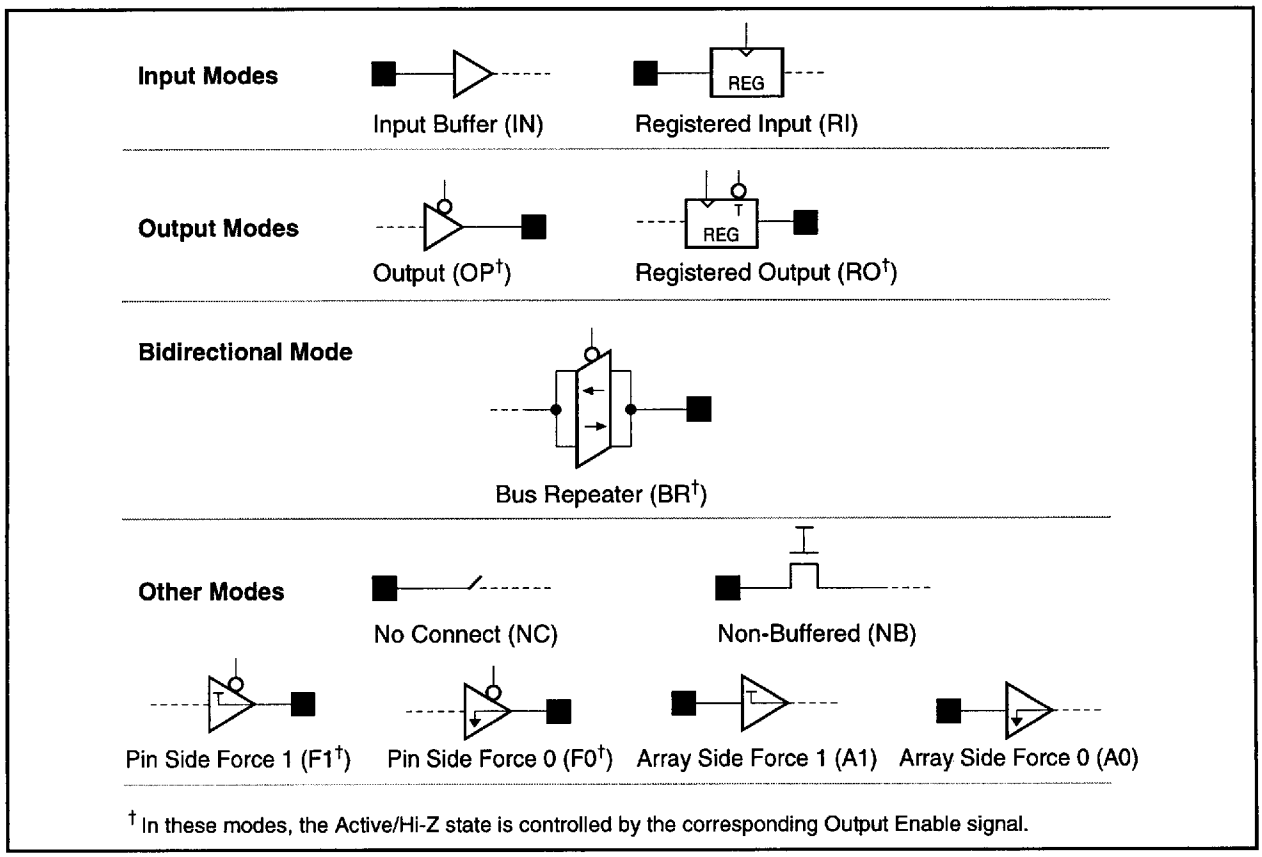


Figure 4: IQ Family I/O Buffer Attributes

I/O Buffer Function	Data Flow	Tristate Function	Mnemonic Used by I-Cube Software
Input	Flow–through	No	IN
	Registered	No	RI
Output	Flow–through	Yes	OP
	Registered	Yes	RO
Bidirectional (Bus Repeater)	Flow–through	Yes	BR
Pin Side Force 0 or 1	N/A	Yes	F0, F1
Array Side Force 0 or 1	N/A	No	A0, A1
Non Buffered	Flow–through	No	NB
No Connect	N/A	N/A	NC

Table 2: Summary of Programmable I/O Attributes for IQ Devices

Output Voltage Level

When an I/O Port is configured in the "output" modes - Output (OP), Registered Output (RO), and Output Force 1 - the output high voltage can be programmed as TTL high or CMOS high. In the Bus Repeater (BR) mode, the output high level is always CMOS high.

Programmable Pull-up Current

As shown in Figure 5, the I/O buffer contains several pull-up devices. The normal pull-up current (I_{OH})is supplied by an n or p channel device for TTL and CMOS output levels respectively. The devices supplying the normal pull-up are controlled by internally generated control signals.

An additional pull-up current (I_{PU-WK}) or (I_{PU-SG}) can be programmed at each I/O Port. This additional current is primarily used for the Bus Repeater (BR) mode, but its use is not restricted to that mode alone. P channel devices, controlled by programming cells are used to supply the additional pull-up current; therefore, when this feature is used with one of the "output" modes - Output (OP), Registered Output (RO), Bus Repeater (BR), and Output Force 1 (F1) - the outputs high voltage levels become CMOS levels.

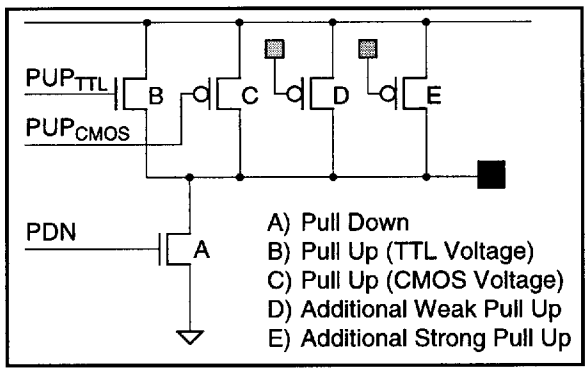


Figure 5: IQ Output Driver and Pull-Up Current

Configuration Controller

The configuration of IQ devices involves initializing internal Mode/Control register, configuring the I/O Ports and establishing connections among the Switch Matrix lines. The IQ devices are ready for configuration as soon as they come out of reset.

The JTAG (IEEE 1149.1) interface, described below is used as the primary configuration mechanism for configuring IQ devices. In addition, the RapidConnect parallel mode is available for changing connections in the Switch Matrix.

JTAG Interface

The JTAG interface is a serial interface and uses four pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). TCK is used to clock data in and out of TDI and TDO. TMS, in conjunction with TDI implements the state machine that controls the various operations of the JTAG protocol. In addition, the device reset signal (TRST*) is used to reset the JTAG controller.

I/O Port Configuration

I/O Port configuration is accomplished by loading the appropriate bit stream into the programming registers present at each I/O Port. Only the JTAG interface can be used to load these programming registers.

Switch Matrix Configuration

The contents of the SRAM cells controlling the Switch Matrix connections can be modified using either the JTAG interface or the RapidConnect interface.

The JTAG serial interface is used to load the data, one word at a time into the SRAM cells in the Switch Matrix. The RapidConnect parallel interface, on the other hand, provides direct write access to individual SRAM cells in the Switch Matrix.

The RapidConnect mode is used in applications which require fast switching. In this mode, a designated number of I/O pins are reassigned as RapidConnect pins. These pins form the address (RA, CA), instruction (C0, C1) and control ($\overline{WE}$, $\overline{STROBE}$) buses. These buses directly address the internal Switch Matrix SRAM cells allowing their contents to be altered very quickly, resulting in fast connection changes. For more details refer to the section on "Rapidconnect Hardware Interface".

Miscellaneous Details

Device Reset

To ensure proper operation, the device reset pin, TRST* must be held low during power up. The recommended reset circuitry is shown in Figure 6.

IQ devices can be reset either by pulsing TRST* low or by applying five JTAG clocks (TCK pin) while holding TMS high.

When the IQ device is reset, the I/O buffers return to the No Connect (NC) state, Turbo mode (see next section) is set to its default state, and the RapidConnect mode is disabled.

When the IQ device is reset, the Switch Matrix SRAM cells are NOT cleared. The SRAM cells must be cleared explicitly by loading the initialization bit stream sequence, which is generated either by the user or by I-Cube supplied software.

The IQ devices are ready for configuration as soon as they come out of reset.

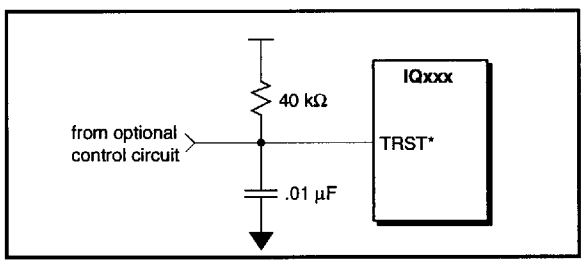


Figure 6: Reset Circuit

Turbo Mode

The Turbo mode reduces the propagation delay "t_{PLH}" and "t_{PHL}" through the IQ devices. This is achieved by detecting low-to-high and high-to-low transitions earlier than the standard mid-voltage threshold. In this mode, the low-to-high transition point is set at a voltage lower that the mid-point $V_{DD}/2$, while the high-to-low transition point is set at a voltage higher than $V_{DD}/2$.

To permit high frequency NRZ data streams to pass through the IQ devices, the Turbo mode can be disabled by changing the appropriate bit in the Mode/Control Register. For further information refer to the Technical Note: "The Turbo Mode".

The Turbo mode is disabled upon reset for all IQ devices except IQ48 and IQ32B, and can be enabled or disabled through JTAG. The initialization sequence generated by the I-Cube software enables the Turbo Mode unless instructed to do otherwise.

In this data sheet, all AC parameters except the NRZ data rate (R_{DATA}) are specified with the Turbo Mode enabled.

Clock and Output Enable Pins

The IQ devices have two global clock pins, ICLK and OCLK. These pins are used as clocks for the I/O Ports configured as Registered Input (RI) and Registered Output (RO) respectively. When unused, these pins should be tied to V_{SS}.

The Output Enable pins are used to control the active and hi-Z states of the I/O Ports configured as Output (OP), Registered Output (RO), Bus Repeater (BR), Pin Side Force 0 (F0) and Pin Side Force 1 (F1). Table 7 lists the I/O Ports controlled by the different Output Enable pins. In these modes, the I/O Port buffers are driving when the corresponding Output Enable signal is low, and hi-Z when it is high. The Output Enable signals have no effect on the I/O Ports configured in any modes other than the ones listed above. In most applications the Output Enable pins will be tied to V_{SS}.

Mode/Control Register

The IQ devices contain a 16-bit register that is used to store the RapidConnect Enable and Turbo Mode Enable bits. The remaining bits are used for internal testing purposes.

Bias Resistors

Three external resistors R_{OD}, R_{ID} and R_{PU} are required for proper operation of the IQ320 and IQ240B. These resistors are connected between the respective pins and V_{ss} and are used to establish internal reference currents. Refer to the Pin Summary table (Table 6) for resistor values. The IQ160, IQ128B, IQ96, IQ64B, IQ48 and the IQ32B do not require these external resistors.

Configuring IQ Devices

The IQ devices are typically configured as follows:

- The device is reset by external circuitry (TRST*=0)
- A bit stream is downloaded through the JTAG interface to initialize the JTAG configuration controller, clear and/or configure the Switch Matrix SRAM cells, configure the I/O Ports and lastly set the Mode/Control register to enable RapidConnect mode and/or disable Turbo Mode if necessary.
- Switch connections are changed with JTAG or RapidConnect (if enabled).

Bit Stream Generation

A bit stream can be generated off-line or in-system by an embedded CPU using one of the following methods:

- By using I-Cube Development System Software products IDS100 or IDS200.
- By using I-Cube's "Programming Library for IQ Devices" software product IDS500, and an embedded processor.
- Generated by the user with the help of the "IQ Family Register Programming User's Reference" manual. I-Cube software is not required when using this method.

If the bit stream is generated off-line then, depending on the application, it is either stored in non-volatile memory or directly downloaded from a host processor.

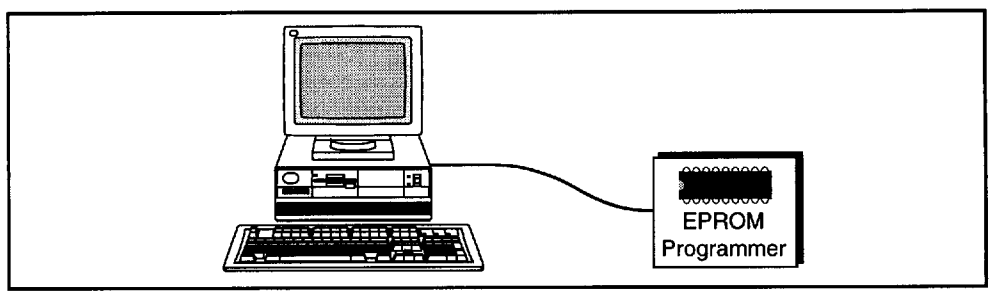


Figure 7: Off -line Bit Stream Generation

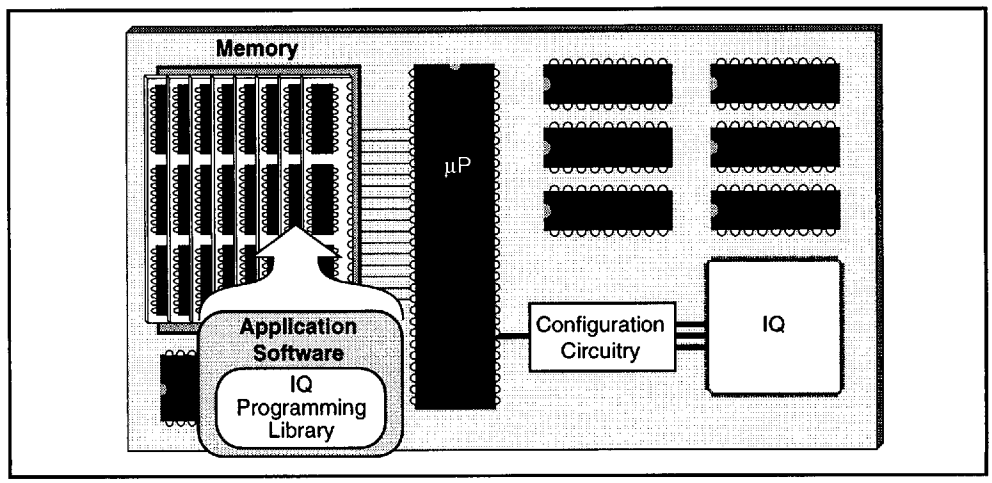


Figure 8: Embedded Bit Stream Generation

JTAG Hardware Interface

JTAG-based configuration allows a single IQ device or multiple IQ devices connected in a chain to be programmed in a single operation. For multiple IQ configuration the TCK, TMS and TRST* signals are bused to all devices. The TDI and TDO signals are daisy chained as shown in Figure 9.

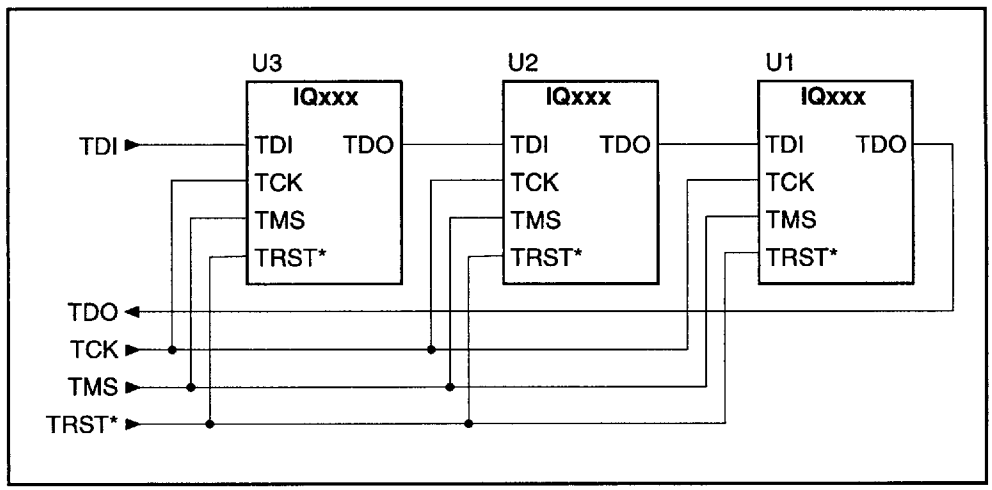


Figure 9: Configuring Multiple IQ Devices

During the initial configuration sequence, the JTAG controllers on all IQ devices are first brought to their default state by either using the TRST* reset pin or by applying a sequence of five 1s ("11111") on the TMS pins (the JTAG reset sequence). This is followed by the actual configuration bit stream, which is downloaded into the IQ devices over the TDI and TMS pins. The JTAG cycle count, configuration times and bit stream size are shown in Table 3.

Operation	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
Make /Break a single connection using JTAG	346 cycles	346 cycles	186 cycles	186 cycles	122 cycles	122 cycles	74 cycles	74 cycles
Configuration Time (µs)	17.3	17.3	9.3	9.3	4.88	4.88	2.96	2.96
Configure all I/O Ports	1306 cycles	1306 cycles	666 cycles	666 cycles	410 cycles	410 cycles	218 cycles	218 cycles
Configuration Time (µs)	65.3	65.3	33.3	33.3	16.4	16.4	8.72	8.72
Complete Configuration [Configure all I/O Ports and Switch Matrix connections]	68,000 cycles	54,000 cycles	22,000 cycles	18,000 cycles	10,000 cycles	8,000 cycles	3,000 cycles	2,500 cycles
Configuration Time (ms)	3.4	2.7	1.1	0.72	0.4	0.32	0.15	0.125
Bit stream size (Bytes)	17,000	13,500	5,500	4,500	2,500	2,000	750	625

Table 3: Number of JTAG Cycles and Configuration Time (using a 20 MHz JTAG Clock)

RapidConnect Hardware Interface

RapidConnect mode allows direct access to the Switch Matrix SRAM cells allowing fast connection changes. By using RapidConnect, a single connection can be changed (made or broken) in one SRAM write cycle. This feature is very useful for real-time switching applications. Figure 10 shows a typical interface for real-time configuration of the IQ devices. Table 4 shows the number of I/O Ports used by the RapidConnect interface.

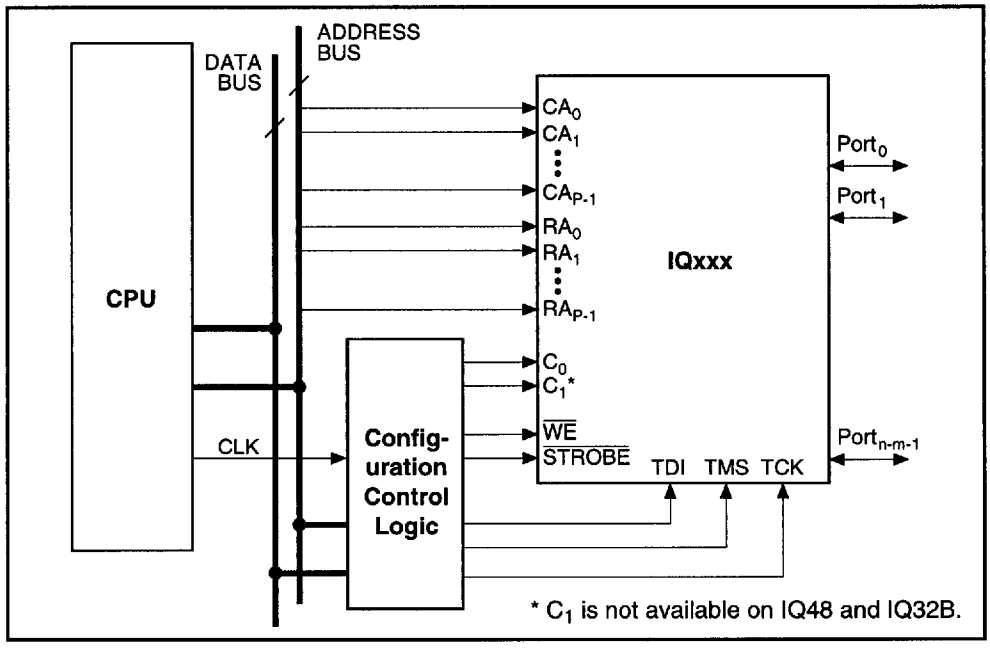


Figure 10: Target System Interface in RapidConnect Mode

	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
Total number of signal I/O Ports on the device (n)	320	240	160	128	96	64	48	32
I/O Ports used for RapidConnect interface (m)	24	24	20	18	18	16	15	13
Number of I/O Ports used for Row and Column Address each (p)	10	10	8	7	7	6	6	5
Number of signal I/O Ports that can be switched using RapidConnect interface (n-m)	296	216	140	102 †	78	48	33	19

Table 4: Number of Pins Used for RapidConnect Interface

† Due to bond-out restrictions, the IQ128B has only (n-m-8) I/O Ports that can be switched using RapidConnect.

RapidConnect Commands and Initialization

Upon reset, the RapidConnect mode is disabled and must be enabled by setting the RapidConnect Enable bit in the on-chip Mode/Control Register. In addition, the RapidConnect interface pins must be configured as inputs (IN). These two operations are performed by loading the appropriate bit stream through the JTAG configuration interface.

Pins used for RapidConnect form three buses - address, control and instruction. As shown in Figure 2, the Switch Matrix SRAM cells form a two dimensional array and each SRAM cell is uniquely identified by its Row Address, RA_0 - RA_{P-1}, and Column Address, CA_0 - CA_{P-1}. The control bus is composed of a write enable (chip select) signal, $\overline{WE}$, and write strobe signal, $\overline{STROBE}$. C0 and C1 comprise the command bus. Table 5 describes various combinations of commands.

C1	C0	RapidConnect Action
0	0	Write "0" to the selected SRAM cell, breaking the connection. Clear all other SRAM cells in the row selected by Row Address, thereby breaking the corresponding connections.
0	1	Write "1" to the selected SRAM cell, making the connection. Clear all other SRAM cells in the row selected by Row Address, thereby breaking the corresponding connections.
1	0	Write "0" to the selected SRAM cell, breaking the connection. No other connections are affected.
1	1	Write "1" to the selected SRAM cell, making the connection. No other connections are affected.

Table 5: RapidConnect Operations

The making or breaking of a connection takes place on the falling edge of $\overline{STROBE}$, when $\overline{WE}$ is active (low).

When RapidConnect is enabled, the JTAG interface can be used to change the I/O Port attributes but cannot be used to change Switch Matrix connections. The RapidConnect mode must first be disabled (through the JTAG interface) before the Switch Matrix connections can be changed using the JTAG interface.

The number of I/O Ports that can be addressed (switched) using the RapidConnect interface is shown in Table 4.

For more application details on the RapidConnect interface, refer to the related Technical Notes in the "Programmable Switching and Interconnect Devices - Applications Handbook".

Pin Summary

The pin summary for the members of the IQ family is given in Tables 6 and 7.

Pin Name								I/O/B	Description
IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B		
P000 - P295	P000 - P215	P000 - P139	P000 - P109	P00 - P77	P00 - P47	P00 - P32	P00 - P18	I/O/B	I/O port pins
P296 - P305/ CA0 - CA9	P216 - P225/ CA0 - CA9	P140 - P147/ CA0 - CA7	P110 - P116/ CA0 - CA6	P78 - P84/ CA0 - CA6	P48 - P53/ CA0 - CA5	P33 - P38/ CA0 - CA5	P19 - P23/ CA0 - CA4	I/O/B	I/O port pins in JTAG serial configuration mode and crossbar column address pins in RapidConnect mode
P306 - P315/ RA0 - RA9	P226 - P235/ RA0 - RA9	P148 - P155/ RA0 - RA7	P117 - P123/ RA0 - RA6	P85 - P91/ RA0 - RA6	P54 - P59/ RA0 - RA5	P39 - P44/ RA0 - RA5	P24 - P28/ RA0 - RA4	I/O/B	I/O port pins in JTAG serial configuration mode and crossbar row address pins in RapidConnect mode
P316/C0	P236/C0	P156/C0	P124/C0	P92/C0	P60/C0	P45/C0	P29/C0	I/O/B	I/O port or RapidConnect control bit 0
P317/C1	P237/C1	P157/C1	P125/C1	P93/C1	P61/C1	-	-	I/O/B	I/O port or RapidConnect control bit 1
P318/$\overline{WE}$	P238/$\overline{WE}$	P158/$\overline{WE}$	P126/$\overline{WE}$	P94/$\overline{WE}$	P62/$\overline{WE}$	P46/$\overline{WE}$	P30/$\overline{WE}$	I/O/B	I/O port or RapidConnect write enable, Active low
P319/$\overline{STROBE}$	P239/$\overline{STROBE}$	P159/$\overline{STROBE}$	P127/$\overline{STROBE}$	P95/$\overline{STROBE}$	P63/$\overline{STROBE}$	P47/$\overline{STROBE}$	P31/$\overline{STROBE}$	I/O/B	I/O port or RapidConnect strobe, Active low
$\overline{OE0}$-$\overline{OE3}$	$\overline{OE0}$-$\overline{OE3}$	$\overline{OE0}$-$\overline{OE3}$	$\overline{OE0}$-$\overline{OE3}$	$\overline{OE0}$-$\overline{OE3}$	$\overline{OE0}$-$\overline{OE3}$	$\overline{OE0}$	$\overline{OE0}$	I	Dedicated output enable control pins. Active low. Each pin controls an equal number of I/O pins. See next table.
ICLK	ICLK	ICLK	ICLK	ICLK	ICLK	ICLK	ICLK	I	Clock for input registers
OCLK	OCLK	OCLK	OCLK	OCLK	OCLK	OCLK	OCLK	I	Clock for output registers
TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	I I O	JTAG pins
TRST*	TRST*	TRST*	TRST*	TRST*	TRST*	TRST*	TRST*	I	Chip Reset, Active low
ROD	ROD	N/A	N/A	N/A	N/A	N/A	N/A	I	External 12K resistor to ground
RID	RID	N/A	N/A	N/A	N/A	N/A	N/A	I	External 12K resistor to ground
RPU	RPU	N/A	N/A	N/A	N/A	N/A	N/A	I	External 18K resistor to ground
				V_{DD}.PAD	V_{DD}.PAD	V_{DD}.PAD	V_{DD}.PAD	P	Power Pins for I/O Buffer Drivers Only
				V_{DD}	V_{DD}	V_{DD}	V_{DD}	P	Power Pins for on-chip circuitry other than I/O Buffer Drivers
V_{DD}	V_{DD}	V_{DD}	V_{DD}					P	Power Pins for both I/O Buffer Drivers and on-chip circuitry
				V_{SS}.PAD	V_{SS}.PAD	V_{SS}.PAD	V_{SS}.PAD	P	Ground Pins for I/O Buffer Drivers Only
				V_{SS}	V_{SS}	V_{SS}	V_{SS}	P	Ground Pins for on-chip circuitry other than I/O Buffer Drivers
V_{SS}	V_{SS}	V_{SS}	V_{SS}					P	Ground Pins for both I/O Buffer Drivers and on-chip circuitry

Table 6: Pin Summary

	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
$\overline{OE0}$	0 -79	0-59	0-39	0-31	0-23	0-15	0-47	0-31
$\overline{OE1}$	80-159	60-119	40-79	32-63	24-47	16-31	-	-
$\overline{OE2}$	160-239	120-179	80-119	64-95	48-71	32-47	-	-
$\overline{OE3}$	240-319	180-239	120-159	96-127	72-95	48-63	-	-

Table 7: Output Enable Pin Summary

Electrical Specifications

Absolute Maximum Ratings (1)

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	-0.3 to +7.0	V
V_{DD}.PAD	Supply Voltage for I/O Buffer Driver (IQ96, IQ64B, IQ48 and IQ32B only)	$-0.3 \le V_{DD}.PAD \le V_{DD} + 0.3$	V
V_{IN} (2)	Input Voltage (IQ320, IQ240B, IQ160 and IQ128B)	-0.3 to V_{DD}+0.3	V
	Input Voltage (IQ96, IQ64B, IQ48 and IQ32B)	-0.3 to V_{DD}.PAD+0.3	V
T_J	Junction Temperature (PQFP, TQFP and PLCC)	150	°C
	Junction Temperature (MQUAD, PBGA and PPGA)	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{SINK}	Sink Current per Pin (All devices except IQ160 and IQ128B)	150	mA
	Sink Current per Pin (IQ160 and IQ128B)	250	mA

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	+4.75 to +5.25	V
V_{DD}.PAD	I/O Buffer Driver Pad Voltage to Ground (IQ96, IQ64B, IQ48 and IQ32B only)	+4.75 to +5.25 or +2.7 to +3.3	V
T_A	Operating Temperature	0 to +70	°C

Capacitance (3)

Symbol	Parameter	IQ320, IQ240B		IQ160, IQ128B		IQ96, IQ64B		IQ48, IQ32B		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
C_{JTAG}	TDI, TMS, TCK and TRST* Pins	-	8	-	8	-	5	-	5	pF
C_{PORT}	I/O Port Pins	-	12	-	12	-	10	-	10	pF
C_{IN}	OE, ICLK, OCLK Pins	-	10	-	10	-	8	-	8	pF

Notes:
(1) Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A maximum overshoot and undershoot of 2V for a maximum duration of 20 ns is acceptable.
(3) Capacitance measured at 25°C. Sample-tested only.

DC Electrical Specifications

(T_A = 0°C to 70°C, V_{DD} = 5V±5%; V_{DD}.PAD = 4.75V to 5.25, or V_{DD}.PAD = 2.7V to 3.3V)

Symbol	Parameter	Conditions	IQ320, IQ240B		IQ160, IQ128B		IQ96, IQ64B		IQ48, IQ32B		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	V_{DD} +0.3	2.0	V_{DD} +0.3	2.0	V_{DD}.PAD +0.3	2.0	V_{DD}.PAD +0.3	V
V_{IL}	Low-Level Input Voltage		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{OH}	High-Level Output Voltage (1)	V_{DD} = Min I_{OH} = -8 mA	2.4	-	2.4	-	-	-	-	-	V
	High-Level Output Voltage (1)	V_{DD} = Min V_{DD}.PAD = 4.75V I_{OH} = -8 mA	NA(7)		NA(7)		2.4	-	2.4	-	V
	High-Level Output Voltage (2)	V_{DD} = Min V_{DD}.PAD = 2.7 V I_{OH} = -4 mA	NA(7)		NA(7)		2.4	-	2.4	-	V
V_{OL}	Low-Level Output Voltage	V_{DD} = Min I_{OL} = 16 mA	-	0.4	-	0.4		-		-	V
	Low-Level Output Voltage	V_{DD} = Min V_{DD}.PAD = 4.75 I_{OL} = 12 mA		NA(7)		NA(7)	-	0.4	-	0.4	V
	Low-Level Output Voltage(3)	V_{DD} = Min V_{DD}.PAD = 2.7 V I_{OL} = 12 mA		NA(7)		NA(7)	-	0.4	-	0.4	V
$\|I_{IH}\|$, $\|I_{IL}\|$	Input Leakage Current for I/O Ports (4)	V_{DD} = Max $0 \le V_{IN} \le V_{DD}$.PAD $\le V_{DD}$	-	5	-	5	-	5	-	5	µA
$\|I_{IH}\|$, $\|I_{IL}\|$	Input Leakage Current for Inputs other than I/O Ports (5)	V_{DD} = Max $0 \le V_{IN} \le V_{DD}$	5	20	5	20	5	20	5	20	µA
$\|I_{OZ}\|$	Tristate Output Off-State Current	V_{DD} = Max $0 \le V_{IN} \le V_{DD}$	-	5	-	5	-	5	-	5	µA
I_{PU-WK}	Programmed-Weak Additional Pull-Up Current	V_{DD} = Min V_O = GND	1.5	2.5	1.5	2.5	2.5	4.5	2.5	4.5	mA
I_{PU-SG}	Programmed-Strong Additional Pull-Up Current	V_{DD} = Min V_O = GND	11	16	11	16	10	15	10	15	mA
I_{OS}	Short Circuit Current (1, 3, 6)	V_{DD} = Max V_O = GND	-60	-	-60	-	-60	-	-60	-	mA
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max V_O = GND	-	8.0	-	3.0	-	3.0	-	1.5	mA
Q_{DDD}	Dynamic Power Supply Current per Input (3)	V_{DD} = Min, No Load, 50% input duty cycle, One output per input	-	0.3	-	0.2	-	0.1	-	0.1	mA/MHz

Notes:
(1) Programmable Output Voltage-level set to TTL.
(2) Programmable Output Voltage-level set to CMOS and no additional pull-up current.
(3) These parameters are guaranteed but not tested in production.
(4) Transient currents of 250 µA are required to pull I/O Ports from logic high to logic low.
(5) Transient currents of 650 µA are required to pull input pins from logic high to logic low.
(6) No more than one output should be tested at a time and the duration of the test should be less than one second.
(7) Not Applicable.

AC Electrical Specifications IQ320, IQ240B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%)
(Assume two I/O Ports connected through the Switch Matrix with 35 pF loading.)

Speed Grade		-12		-15		-20		Units	Ref. Timing Diagram
Symbol	Parameter	Min	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay	-	12.5	-	15	-	20	ns	
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)	-	1	-	1	-	1	ns	
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode	-	0.5	-	0.5	-	0.5	ns	1
$t_{\Delta CMOS}$	Additional Delay when Output Voltage Level is CMOS	-	1	-	1	-	1	ns	
t_{SK}	Skew Between Output Ports (1)	-	1.5	-	1.5	-	1.5	ns	
R_{DATA}	NRZ Data Rate (1)	-	133	-	100	-	80	Mbs	
t_{W+}	Positive Input Signal Pulse Width	7	-	9	-	11	-	ns	
t_{W-}	Negative Input Signal Pulse Width	8	-	11	-	13	-	ns	
t_{PZL}, t_{PZH}	Output Enable to Data Valid	-	12.5	-	15	-	20	ns	2
t_{PLZ}, t_{PHZ}	Output Enable to Output at High Z (1)	-	12.5	-	15	-	20	ns	
f_{RI}	Register Input 4Clock Frequency (1)	-	80	-	66	-	50	MHz	
t_{W-RI}	Register Input Clock Pulse Width, Low or High	5.5	-	6.5	-	9	-	ns	
t_{S-RI}	Register Input Setup Time	0	-	0	-	0	-	ns	3
t_{H-RI}	Register Input Hold Time	2.5	-	2.5	-	2.5	-	ns	
t_{P-RI}	Register Input Clock to Output Data Valid	-	18.5	-	22	-	28	ns	
f_{RO}	Register Output Clock Frequency (1)	-	80	-	66	-	50	MHz	
t_{W-RO}	Register Output Clock Pulse Width, Low or High	5.5	-	6.5	-	9	-	ns	
t_{S-RO}	Register Output Setup Time	6	-	7	-	9	-	ns	4
t_{H-RO}	Register Output Hold Time	0	-	0	-	0	-	ns	
t_{P-RO}	Register Output Clock to Output Data Valid	-	12.5	-	15	-	20	ns	
f_{RIO}	Register Input/Output Clock Frequency (1)	-	80	-	66	-	50	MHz	
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	5.5	-	6.5	-	9	-	ns	
t_{S-RIO}	Register Input/Output Setup Time	0	-	0	-	0	-	ns	
t_{H-RIO}	Register Input/Output Hold Time	2.5	-	2.5	-	2.5	-	ns	5
t_{P-RIO}	Register Input/Output Clock to Output Data Valid	-	12.5	-	15	-	20	ns	
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)	10	-	12	-	15	-	ns	
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)	-	5	-	5	-	5	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency	-	20	-	20	-	20	MHz	
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20	-	20	-	20	-	ns	
t_{S-JTAG}	JTAG Setup Time	15	-	15	-	15	-	ns	6
t_{H-JTAG}	JTAG Hold Time	15	-	15	-	15	-	ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15	-	15	-	15	-	ns	
T_{RC}	RapidConnect Strobe Period	30	-	35	-	40	-	ns	
t_{W-RC}	RapidConnect Strobe Pulse Width	12	-	15	-	18	-	ns	
t_{S-RC}	RapidConnect Address and Data Setup Time	8	-	10	-	12	-	ns	7
t_{H-RC}	RapidConnect Address and Data Hold Time	0	-	0	-	0	-	ns	
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection	35	-	42	-	50	-	ns	

Note:
(1) These parameters are guaranteed but not tested in production.

AC Electrical Specifications IQ160, IQ128B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%)
(Assume two I/O Ports connected through the Switch Matrix with 35 pF loading.)

Speed Grade		-10		-12		-15		-20		Units	Ref. Timing Diagram
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay	-	10	-	12.5	-	15	-	20	ns	
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)	-	1	-	1	-	1	-	1	ns	
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode	-	0.5	-	0.5	-	0.5	-	0.5	ns	1
$t_{\Delta CMOS}$	Additional Delay when Output Voltage Level is CMOS	-	1	-	1	-	1	-	1	ns	
t_{SK}	Skew Between Output Ports (1)	-	1.5	-	1.5	-	1.5	-	1.5	ns	
R_{DATA}	NRZ Data Rate (1)	-	160	-	133	-	100	-	80	Mbs	
t_{W+}	Positive Input Signal Pulse Width	7	-	8.5	-	11	-	13	-	ns	
t_{W-}	Negative Input Signal Pulse Width	5.5	-	6.5	-	9.0	-	11	-	ns	
t_{PZL}, t_{PZH}	Output Enable to Data Valid	-	12	-	14.5	-	17	-	22	ns	2
t_{PLZ}, t_{PHZ}	Output Enable to Output at High Z (1)	-	12	-	14.5	-	17	-	22	ns	
f_{RI}	Register Input Clock Frequency (1)	-	100	-	80	-	66	-	50	MHz	
t_{W-RI}	Register Input Clock Pulse Width, Low or High	4.5	-	5.5	-	6.5	-	8.5	-	ns	
t_{S-RI}	Register Input Setup Time	0	-	0	-	0	-	0	-	ns	3
t_{H-RI}	Register Input Hold Time	2.5	-	2.5	-	2.5	-	2.5	-	ns	
t_{P-RI}	Register Input Clock to Output Data Valid	-	16	-	18.5	-	22	-	28	ns	
f_{RO}	Register Output Clock Frequency (1)	-	100	-	80	-	66	-	50	MHz	
t_{W-RO}	Register Output Clock Pulse Width, Low or High	4.5	-	5.5	-	6.5	-	8.5	-	ns	
t_{S-RO}	Register Output Setup Time	5	-	6	-	7	-	9	-	ns	4
t_{H-RO}	Register Output Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RO}	Register Output Clock to Output Data Valid	-	10	-	12.5	-	15	-	20	ns	
f_{RIO}	Register Input/Output Clock Frequency (1)	-	100	-	80	-	66	-	50	MHz	
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	4.5	-	5.5	-	6.5	-	8.5	-	ns	
t_{S-RIO}	Register Input/Output Setup Time	0	-	0	-	0	-	0	-	ns	
t_{H-RIO}	Register Input/Output Hold Time	2.5	-	2.5	-	2.5	-	2.5	-	ns	5
t_{P-RIO}	Register Input/Output Clock to Output Data Valid	-	10	-	12.5	-	15	-	20	ns	
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)	8	-	10	-	12	-	15	-	ns	
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)	-	4	-	4	-	4	-	4	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency	-	20	-	20	-	20	-	20	MHz	
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20	-	20	-	20	-	20	-	ns	
t_{S-JTAG}	JTAG Setup Time	15	-	15	-	15	-	15	-	ns	6
t_{H-JTAG}	JTAG Hold Time	15	-	15	-	15	-	15	-	ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15	-	15	-	15	-	15	-	ns	
T_{RC}	RapidConnect Strobe Period	30	-	35	-	40	-	40	-	ns	
t_{W-RC}	RapidConnect Strobe Pulse Width	12	-	15	-	18	-	18	-	ns	
t_{S-RC}	RapidConnect Address and Data Setup Time	8	-	10	-	12	-	12	-	ns	7
t_{H-RC}	RapidConnect Address and Data Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection	20	-	25	-	30	-	30	-	ns	

Note:
(1) These parameters are guaranteed but not tested in production.

AC Electrical Specifications IQ96, IQ64B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%, V_{DD}.PAD = 5V±5% or V_{DD}.PAD = 3V±10%)
(Assume two I/O Ports connected through the Switch Matrix with 35 pF loading.)

	Speed Grade	-6		-10		-12		-15		Units	Ref. Timing Diagram
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay	-	6	-	10	-	12.5	-	15	ns	1
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)	-	0.25	-	0.25	-	0.25	-	0.25	ns	
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode	-	0	-	0	-	0	-	0	ns	
$t_{\Delta CMOS}$	Additional Delay when Output Voltage Level is CMOS	-	0.5	-	0.5	-	0.5	-	0.5	ns	
t_{SK}	Skew Between Output Ports (1)	-	1.0	-	1.0	-	1.0	-	1.0	ns	
R_{DATA}	NRZ Data Rate (1)	-	200	-	160	-	133	-	100	Mbs	
t_{W+}	Positive Input Signal Pulse Width	6	-	7	-	8.5	-	11	-	ns	
t_{W-}	Negative Input Signal Pulse Width	4	-	5.5	-	6.5	-	9	-	ns	
t_{PZL}, t_{PZH}	Output Enable to Data Valid	-	8	-	12	-	14.5	-	17	ns	2
t_{PLZ}, t_{PHZ}	Output Enable to Output at High Z (1)	-	8	-	12	-	14.5	-	17	ns	
f_{RI}	Register Input Clock Frequency (1)	-	125	-	100	-	80	-	66	MHz	3
t_{W-RI}	Register Input Clock Pulse Width, Low or High	3.5	-	4.5	-	5.5	-	6.5	-	ns	
t_{S-RI}	Register Input Setup Time	1	-	1	-	1	-	1	-	ns	
t_{H-RI}	Register Input Hold Time	1	-	1	-	1	-	1	-	ns	
t_{P-RI}	Register Input Clock to Output Data Valid	-	10	-	14	-	16.5	-	19	-	
f_{RO}	Register Output Clock Frequency (1)	-	125	-	100	-	80	-	66	MHz	4
t_{W-RO}	Register Output Clock Pulse Width, Low or High	3.5	-	4.5	-	5.5	-	6.5	-	ns	
t_{S-RO}	Register Output Setup Time	4	-	5	-	6	-	7	-	ns	
t_{H-RO}	Register Output Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RO}	Register Output Clock to Output Data Valid	-	7.5	-	11.5	-	14	-	16.5	ns	
f_{RIO}	Register Input/Output Clock Frequency (1)	-	125	-	100	-	80	-	66	MHz	5
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	3.5	-	4.5	-	5.5	-	6.5	-	ns	
t_{S-RIO}	Register Input/Output Setup Time	1	-	1	-	1	-	1	-	ns	
t_{H-RIO}	Register Input/Output Hold Time	1	-	1	-	1	-	1	-	ns	
t_{P-RIO}	Register Input/Output Clock to Output Data Valid	-	7.5	-	11.5	-	14	-	16.5	ns	
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)	6	-	8	-	10	-	12	-	ns	
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)	-	3	-	3	-	3	-	3	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency	-	25	-	25	-	25	-	25	MHz	6
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20	-	20	-	20	-	20	-	ns	
t_{S-JTAG}	JTAG Setup Time	15	-	15	-	15	-	15	-	ns	
t_{H-JTAG}	JTAG Hold Time	15	-	15	-	15	-	15	-	ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15	-	15	-	15	-	15	-	ns	
T_{RC}	RapidConnect Strobe Period	25	-	30	-	35	-	40	-	ns	7
t_{W-RC}	RapidConnect Strobe Pulse Width	10	-	12	-	15	-	18	-	ns	
t_{S-RC}	RapidConnect Address and Data Setup Time	5	-	8	-	10	-	12	-	ns	
t_{H-RC}	RapidConnect Address and Data Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection	18	-	20	-	25	-	30	-	ns	

Note:
(1) These parameters are guaranteed but not tested in production.

AC Electrical Specifications IQ48, IQ32B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%, V_{DD}.PAD = 5V±5% or V_{DD}.PAD = 3V±10%)
(Assume two I/O Ports connected through the Switch Matrix with 35 pF loading.)

Speed Grade		-5		-10		-12		-15		Units	Ref. Timing Diagram
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay	-	5	-	7.5	-	10	-	12.5	ns	
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)	-	0.25	-	0.25	-	0.25	-	0.25	ns	
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode	-	0	-	0	-	0	-	0	ns	1
$t_{\Delta CMOS}$	Additional Delay when Output Voltage Level is CMOS	-	0.5	-	0.5	-	0.5	-	0.5	ns	
t_{SK}	Skew Between Output Ports (1)	-	1.5	-	1.5	-	1.5	-	1.5	ns	
R_{DATA}	NRZ Data Rate (1)	-	250	-	200	-	160	-	133	Mbs	
t_{W+}	Positive Input Signal Pulse Width	5	-	6	-	7	-	8.5	-	ns	
t_{W-}	Negative Input Signal Pulse Width	3	-	4	-	5.5	-	6.5	-	ns	
t_{PZL}, t_{PZH}	Output Enable to Data Valid	-	6	-	8.5	-	11	-	13.5	ns	2
t_{PLZ}, t_{PHZ}	Output Enable to Output at High Z (1)	-	6	-	8.5	-	11	-	13.5	ns	
f_{RI}	Register Input Clock Frequency (1)	-	150	-	125	-	100	-	80	MHz	
t_{W-RI}	Register Input Clock Pulse Width, Low or High	3	-	3.5	-	4.5	-	5.5	-	ns	
t_{S-RI}	Register Input Setup Time	1	-	1	-	1	-	1	-	ns	3
t_{H-RI}	Register Input Hold Time	1	-	1	-	1	-	1	-	ns	
t_{P-RI}	Register Input Clock to Output Data Valid	-	10	-	12	-	14	-	16.5	ns	
f_{RO}	Register Output Clock Frequency (1)	-	150	-	125	-	100	-	80	MHz	
t_{W-RO}	Register Output Clock Pulse Width, Low or High	3	-	3.5	-	4.5	-	5.5	-	ns	
t_{S-RO}	Register Output Setup Time	3.5	-	4	-	5	-	6	-	ns	4
t_{H-RO}	Register Output Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RO}	Register Output Clock to Output Data Valid	-	6	-	8.5	-	11	-	13.5	ns	
f_{RIO}	Register Input/Output Clock Frequency (1)	-	150	-	125	-	100	-	80	MHz	
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	3	-	3.5	-	4.5	-	5.5	-	ns	
t_{S-RIO}	Register Input/Output Setup Time	1	-	1	-	1	-	1	-	ns	
t_{H-RIO}	Register Input/Output Hold Time	1	-	1	-	1	-	1	-	ns	5
t_{P-RIO}	Register Input/Output Clock to Output Data Valid	-	6	-	8.5	-	11	-	13.5	ns	
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)	5	-	6	-	8	-	10	-	ns	
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)	-	3	-	3	-	3	-	3	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency	-	25	-	25	-	25	-	25	MHz	
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20	-	20	-	20	-	20	-	ns	
t_{S-JTAG}	JTAG Setup Time	15	-	15	-	15	-	15	-	ns	6
t_{H-JTAG}	JTAG Hold Time	15	-	15	-	15	-	15	-	ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15	-	15	-	15	-	15	-	ns	
T_{RC}	RapidConnect Strobe Period	20	-	30	-	35	-	40	-	ns	
t_{W-RC}	RapidConnect Strobe Pulse Width	8	-	12	-	15	-	18	-	ns	
t_{S-RC}	RapidConnect Address and Data Setup Time	5	-	8	-	10	-	12	-	ns	7
t_{H-RC}	RapidConnect Address and Data Hold Time	0	-	0	-	0	-	0	-	ns	
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection	16	-	20	-	25	-	30	-	ns	

Notes:
(1) These parameters are guaranteed but not tested in production.

Test Circuit and Timing Diagrams

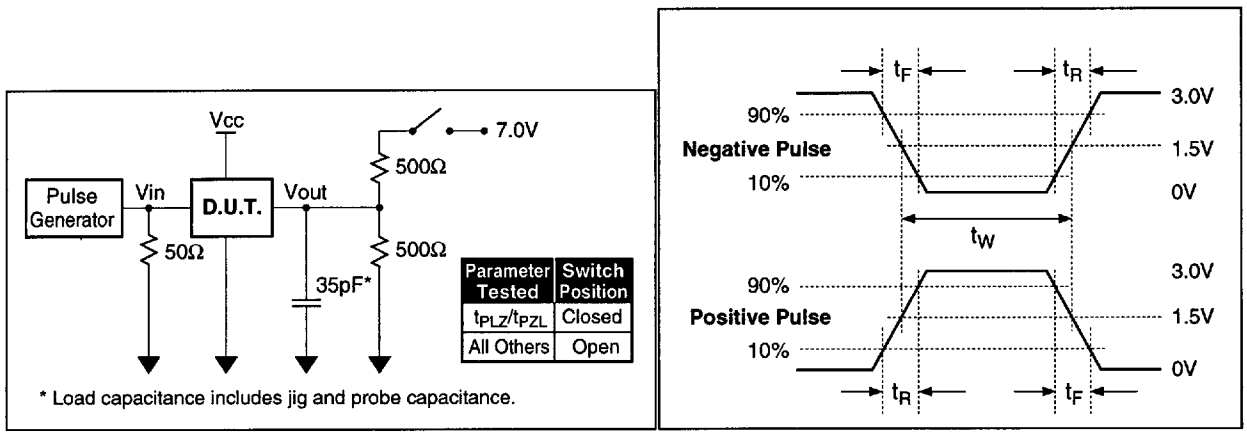
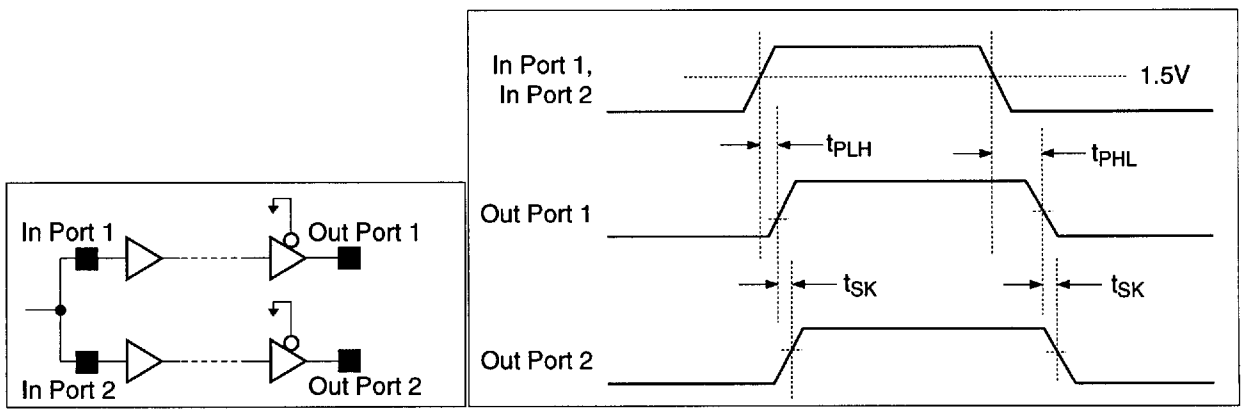
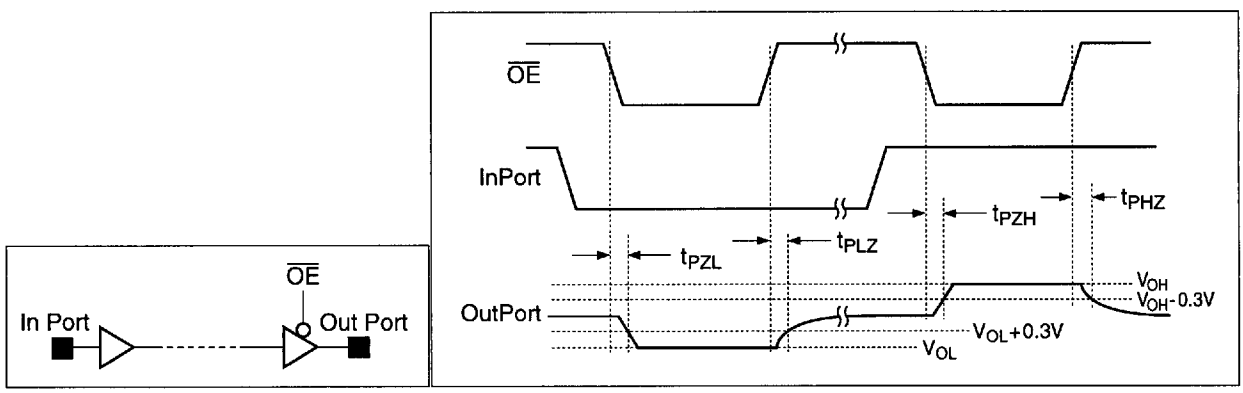


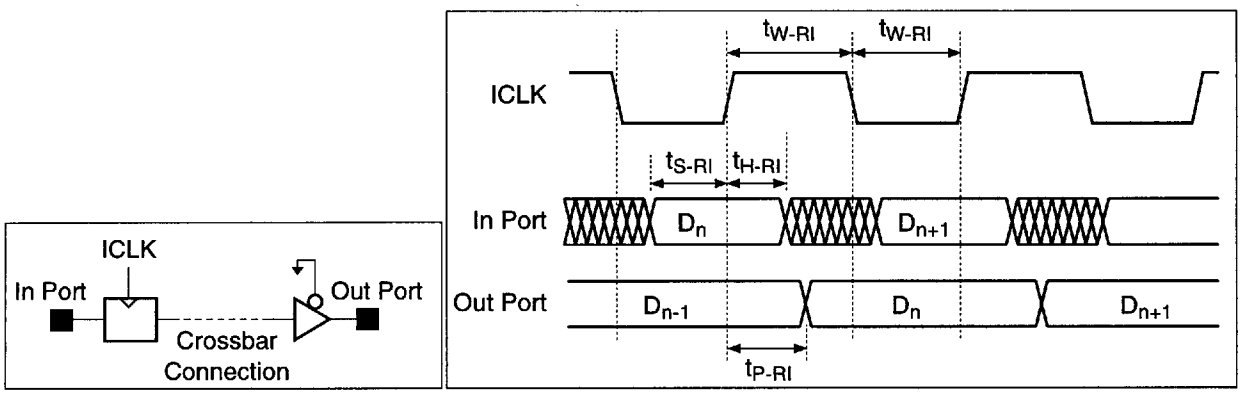
Figure 11: Test Circuit and Waveform Definition



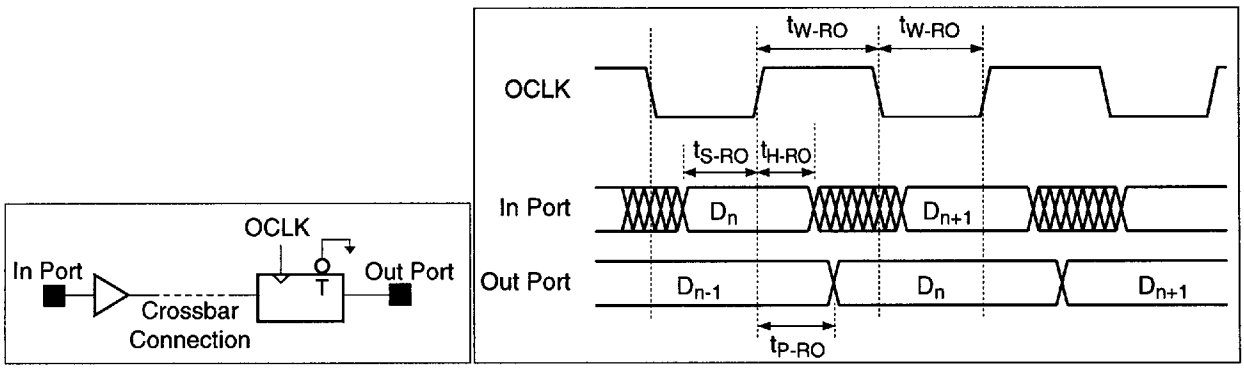
Timing Diagram 1: I/O Port Timing (Flow-through Mode)



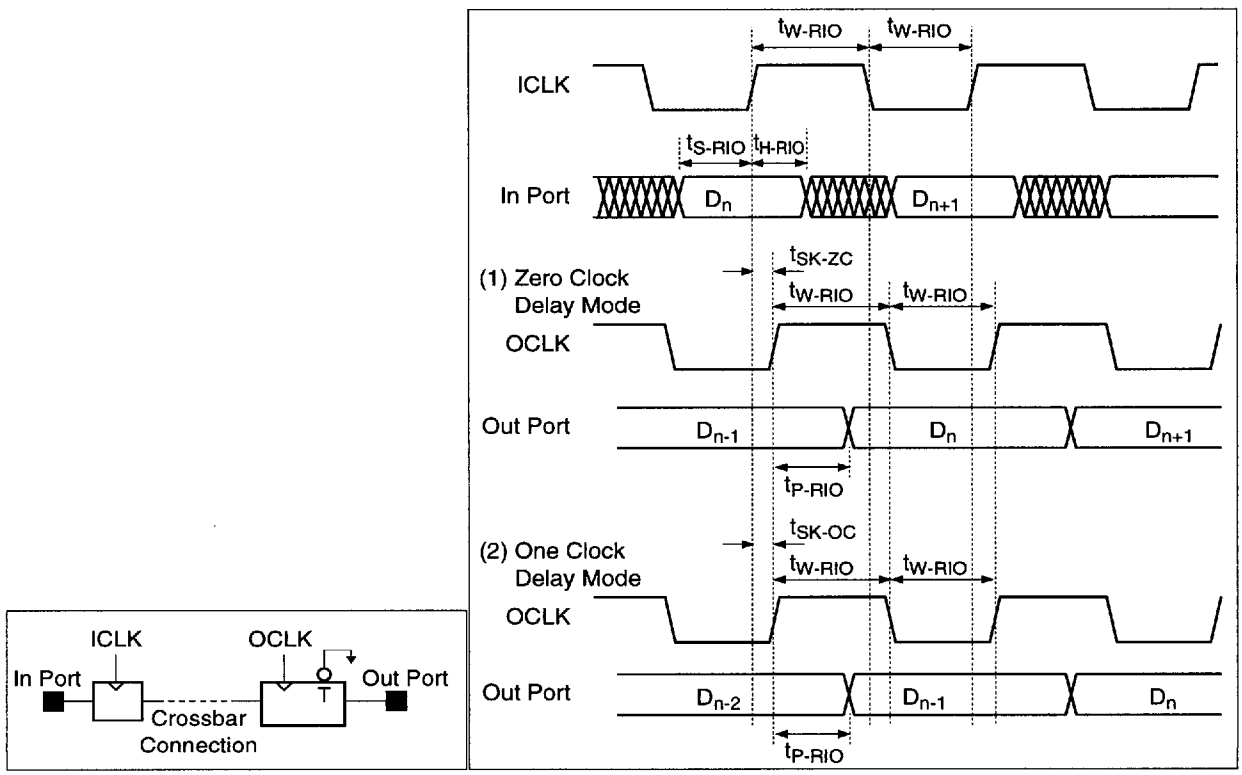
Timing Diagram 2: Output Enable Timing (Flow-through Mode)



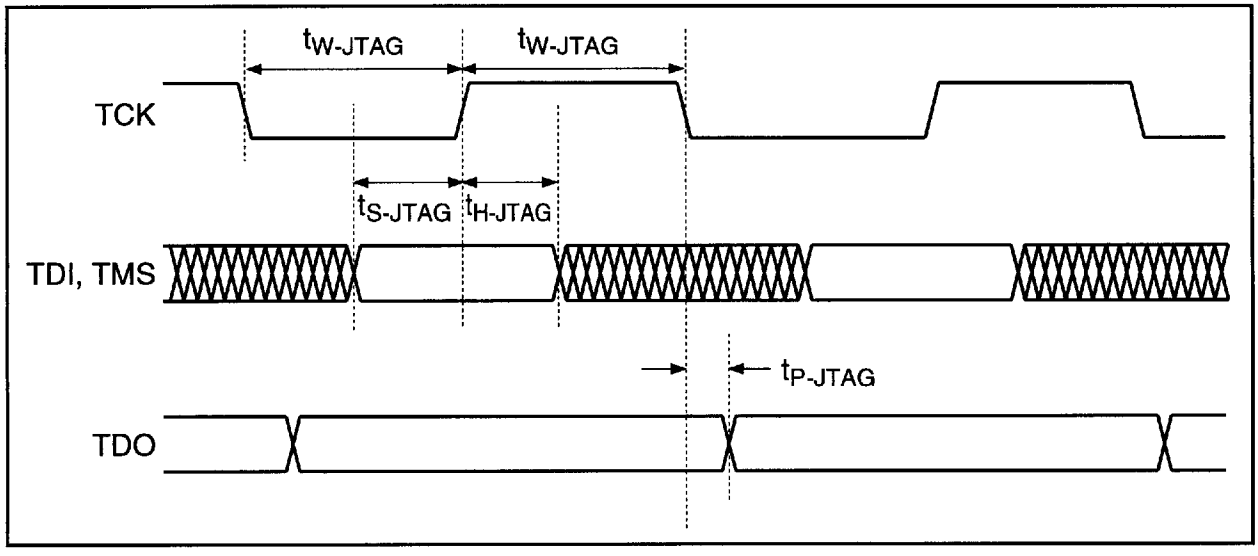
Timing Diagram 3: Clocked Input to Unclocked Output



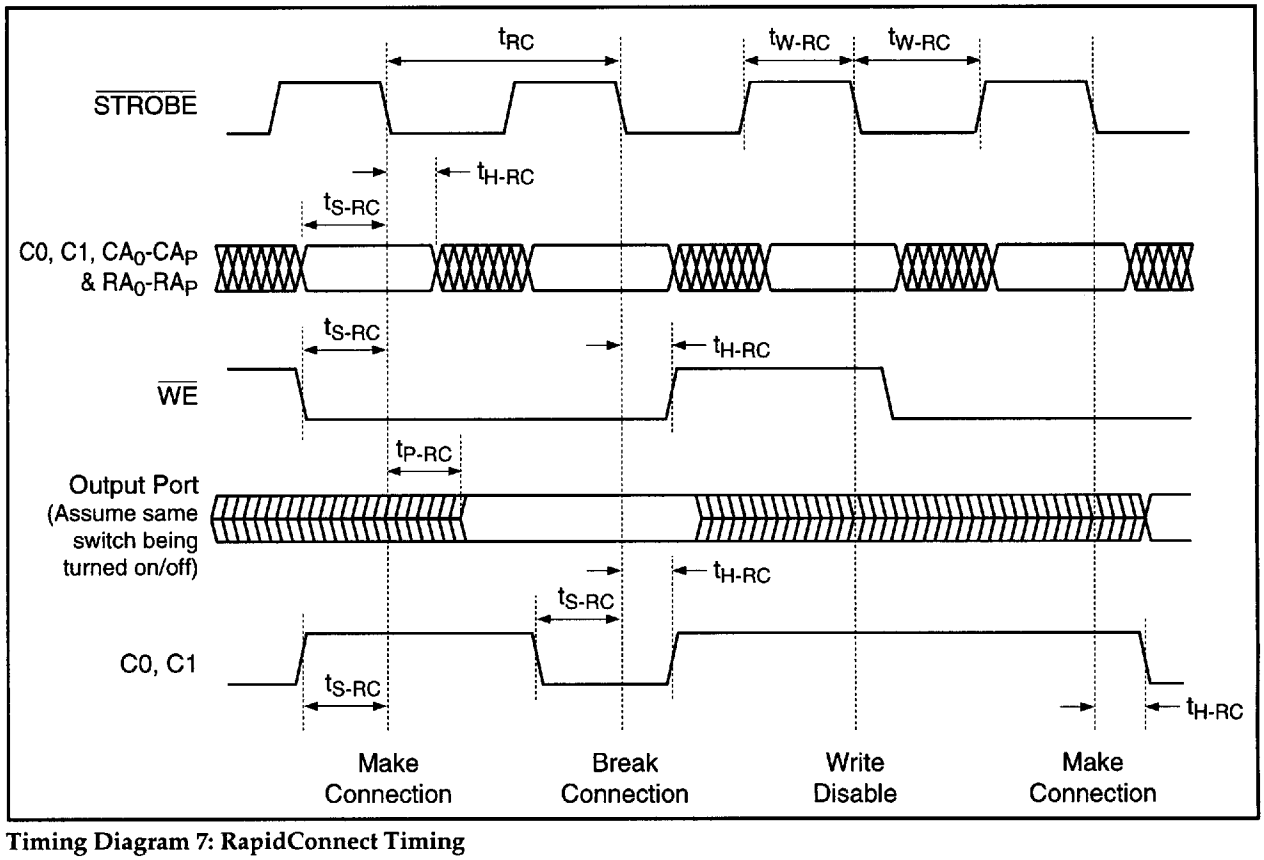
Timing Diagram 4: Unclocked Input to Clocked Output



Timing Diagram 5: Clocked Input to Clocked Output (ICLK and OCLK are Synchronized)

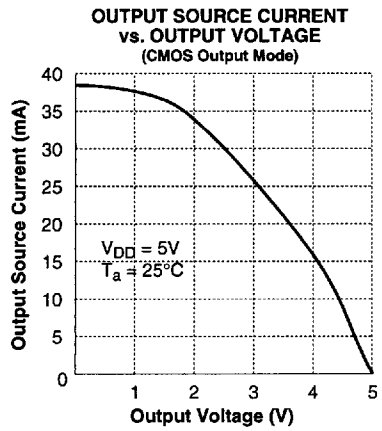


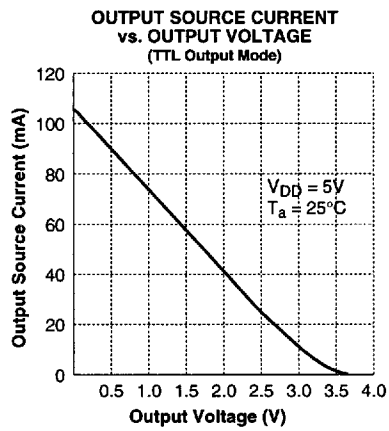
Timing Diagram 6: JTAG Timing

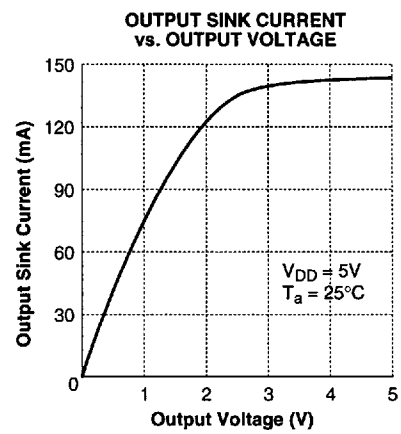


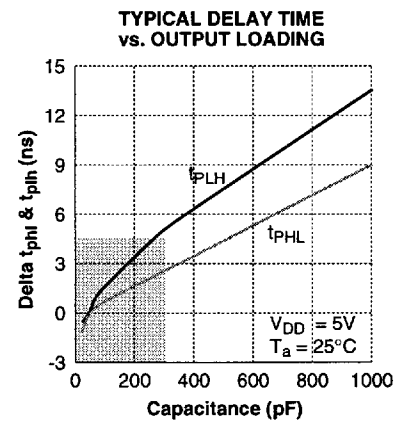
Timing Diagram 7: RapidConnect Timing

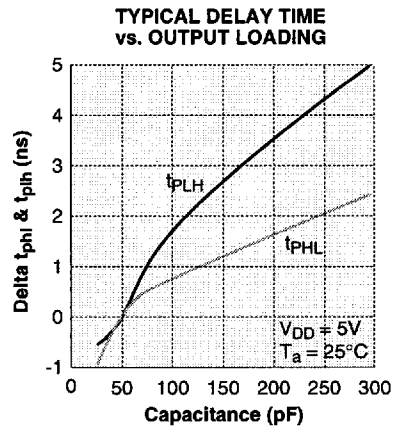
Typical AC and DC Characteristics (Measured for IQ320 and IQ240B)

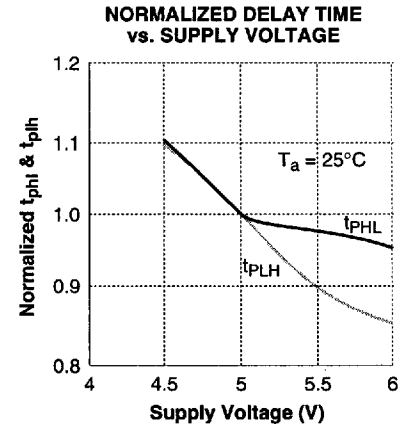


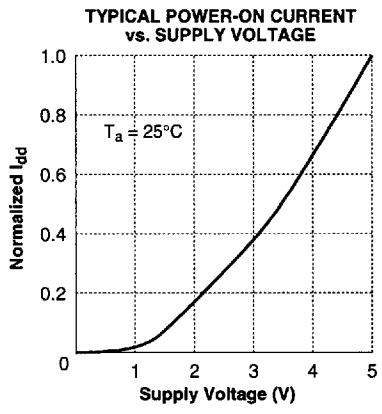


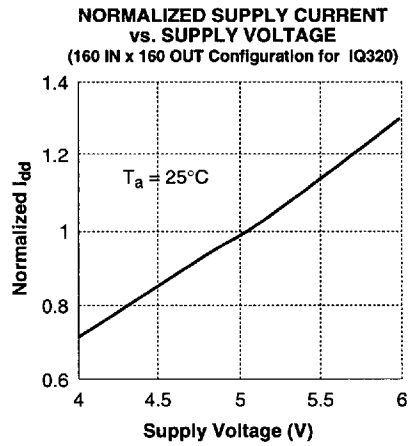


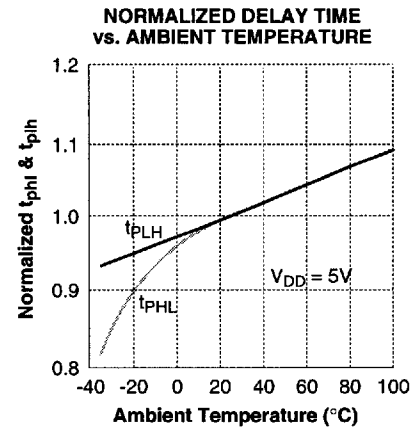






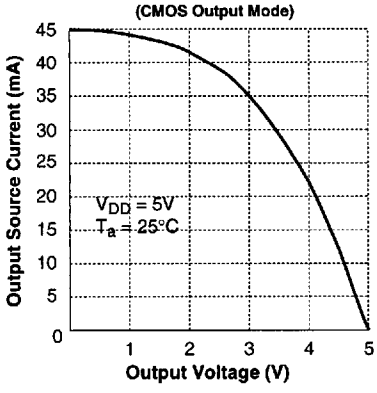




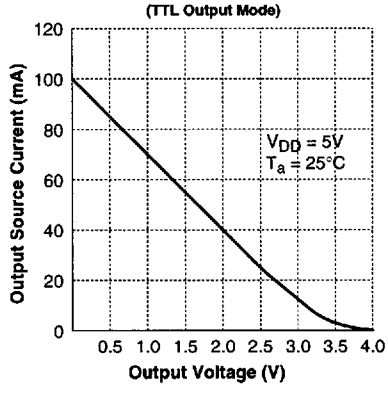


Typical AC and DC Characteristics (Measured for IQ160 and 128B)

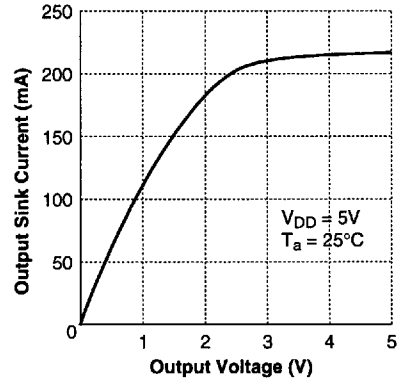
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (CMOS Output Mode)



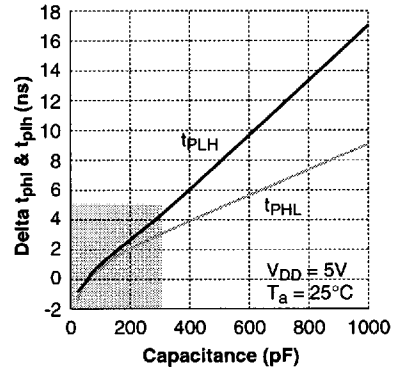
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TTL Output Mode)



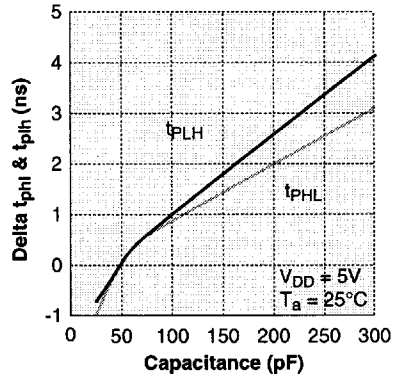
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



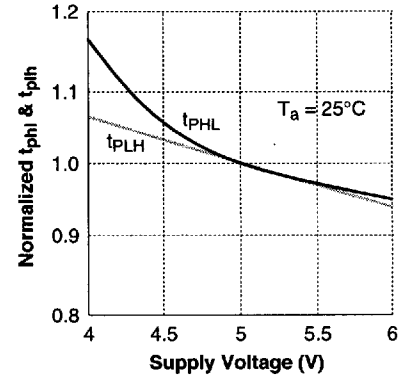
TYPICAL DELAY TIME vs. OUTPUT LOADING



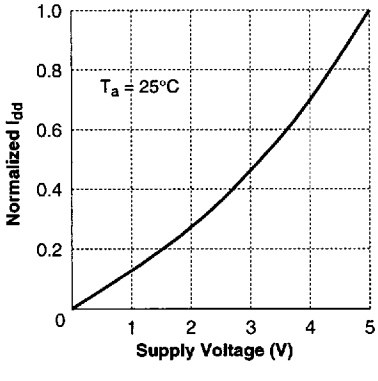
TYPICAL DELAY TIME vs. OUTPUT LOADING



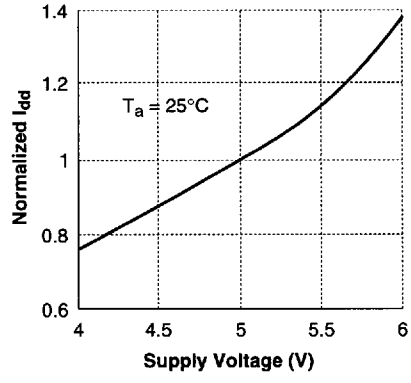
NORMALIZED DELAY TIME vs. SUPPLY VOLTAGE



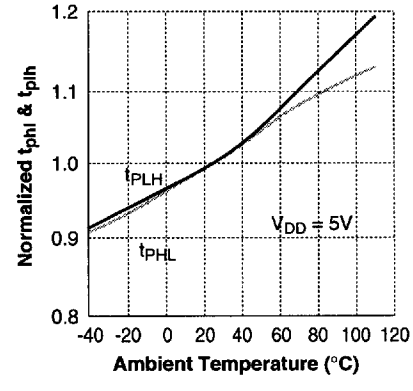
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE (80 IN x 80 OUT Configuration for IQ160)

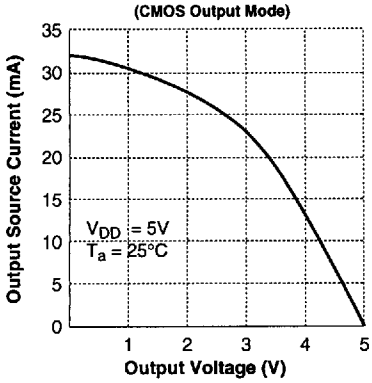


NORMALIZED DELAY TIME vs. AMBIENT TEMPERATURE

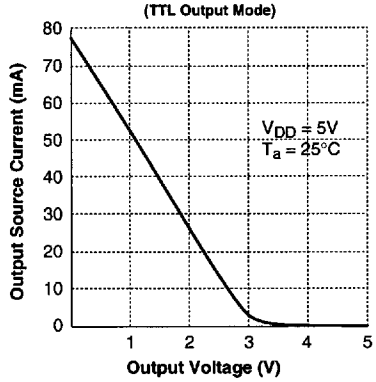


Typical AC and DC Characteristics (Measured for IQ96 and IQ64B)

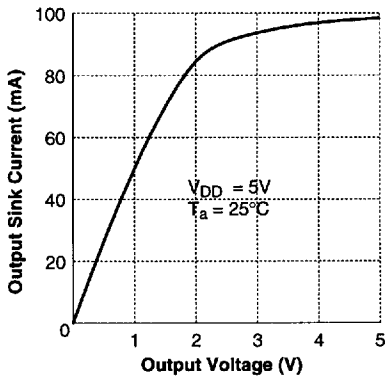
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (CMOS Output Mode)



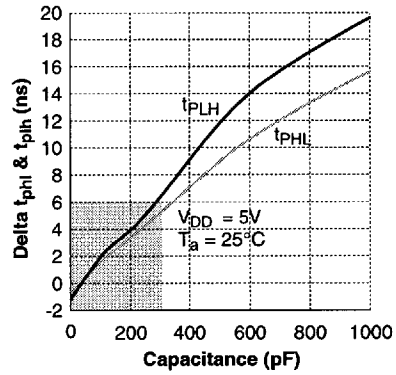
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TTL Output Mode)



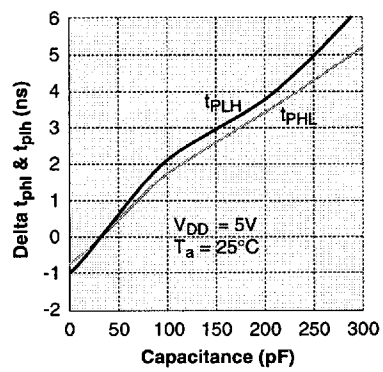
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



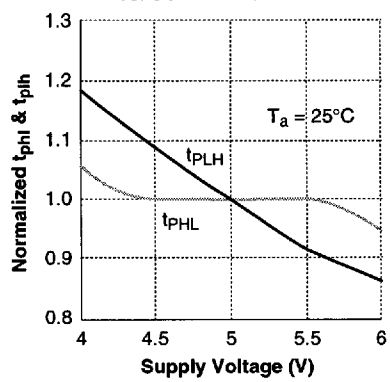
TYPICAL DELAY TIME vs. OUTPUT LOADING



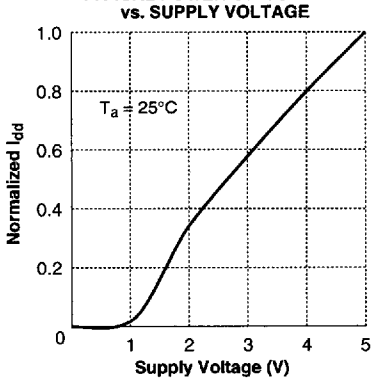
TYPICAL DELAY TIME vs. OUTPUT LOADING



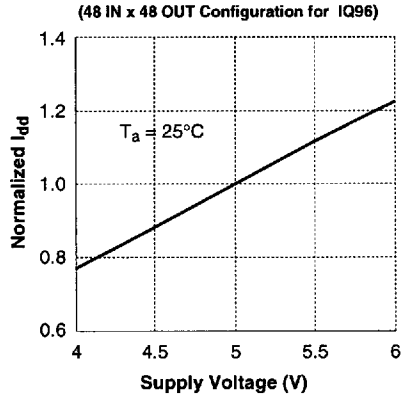
NORMALIZED DELAY TIME vs. SUPPLY VOLTAGE



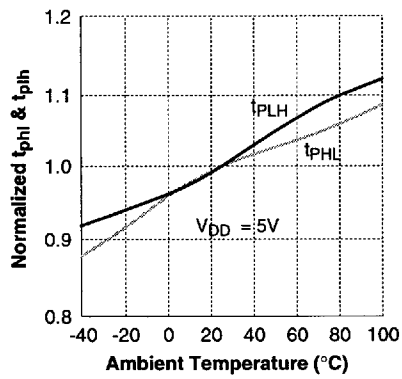
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



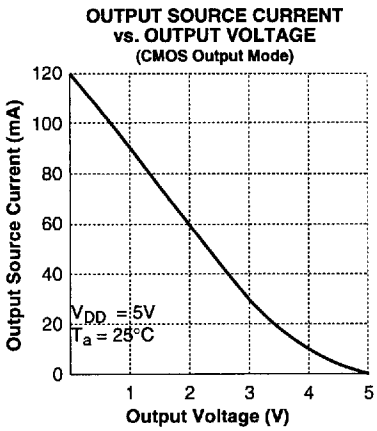
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE (48 IN x 48 OUT Configuration for IQ96)

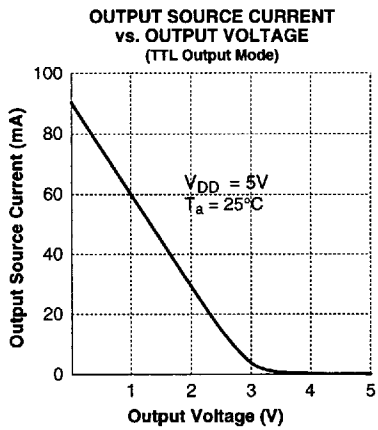


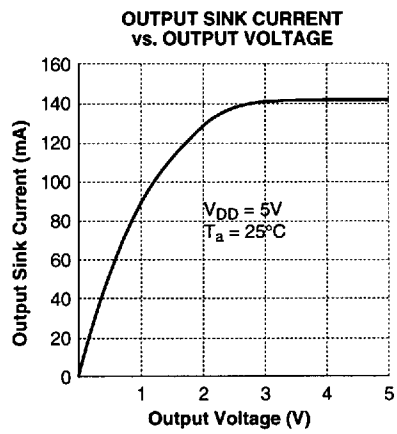
NORMALIZED DELAY TIME vs. AMBIENT TEMPERATURE

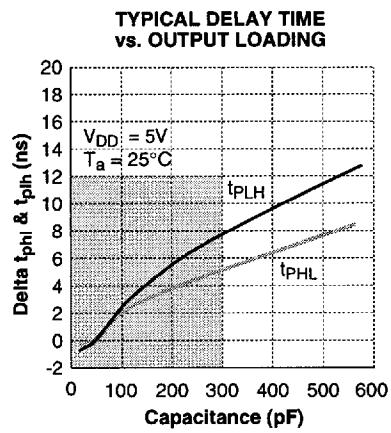


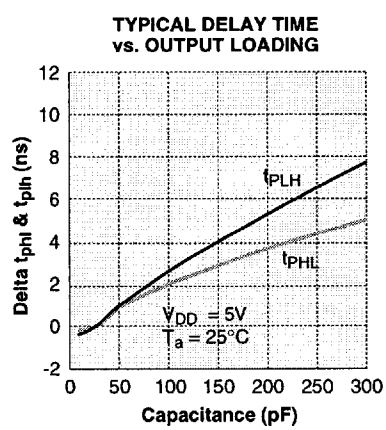
Typical AC and DC Characteristics (Measured for IQ48 and 32B)

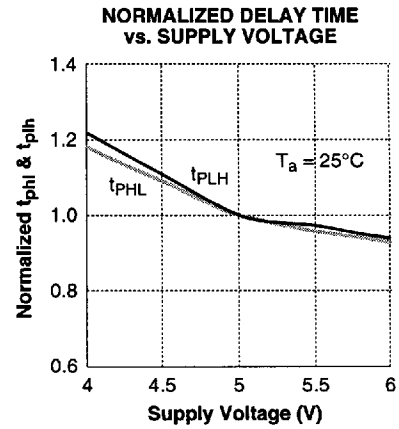


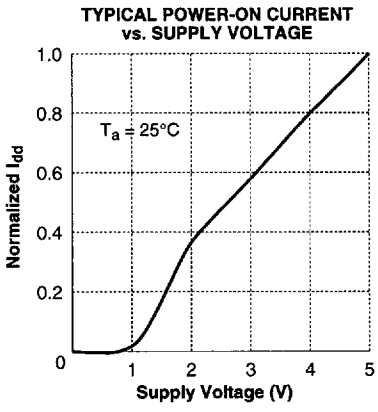


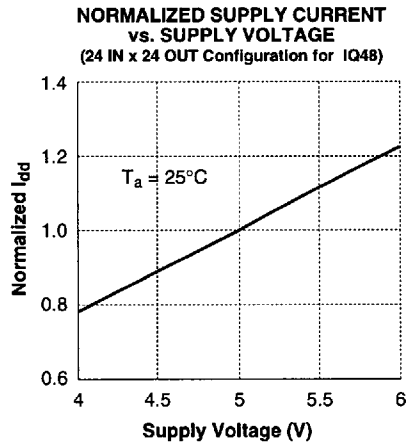


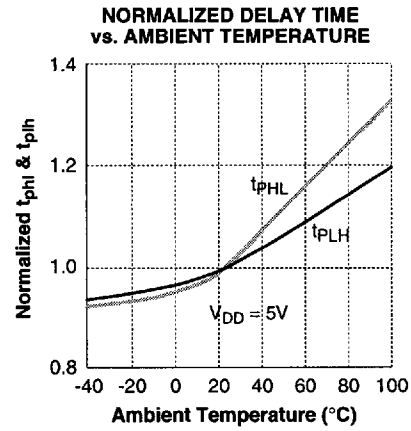












Pinout

IQ320 [PPGA/391L] Package Pinout by Name

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
NC	K4	P043	F20	P093	L31	P143	AE31	P193	AK20	P243	AP2	P293	R5	V_{DD}	AR27
ICLK	K6	P044	C21	P094	K34	P144	AK34	P194	AP20	P244	AH6	P294	M2	V_{DD}	AR3
OCLK	J5	P045	E21	P095	M30	P145	AE29	P195	AL19	P245	AM4	P295	R7	V_{DD}	AR31
$\overline{OE0}$	C33	P046	B22	P096	L33	P146	AK32	P196	AN19	P246	AK2	P296/CA0	N3	V_{DD}	AR35
$\overline{OE1}$	G31	P047	G21	P097	N29	P147	AF32	P197	AJ19	P247	AM2	P297/CA1	P4	V_{DD}	AR7
$\overline{OE2}$	AN3	P048	B24	P098	M32	P148	AL33	P198	AR19	P248	AJ3	P298/CA2	K2	V_{DD}	C35
$\overline{OE3}$	AJ5	P049	D22	P099	N31	P149	AF30	P199	AM18	P249	AK4	P299/CA3	P6	V_{DD}	E1
P000	F8	P050	C23	P100	M34	P150	AM34	P200	AP18	P250	AG7	P300/CA4	L3	V_{DD}	G35
P001	B6	P051	F22	P101	P30	P151	AG31	P201	AK18	P251	AL3	P301/CA5	N5	V_{DD}	J1
P002	C7	P052	B26	P102	N33	P152	AL31	P202	AN17	P252	AG5	P302/CA6	H2	V_{DD}	L35
P003	G9	P053	E23	P103	P32	P153	AG29	P203	AL17	P253	AH4	P303/CA7	N7	V_{DD}	N1
P004	E9	P054	C25	P104	P34	P154	AK30	P204	AR17	P254	AH2	P304/CA8	J3	V_{DD}	R35
P005	B8	P055	G23	P105	R29	P155	AH30	P205	AJ17	P255	AF6	P305/CA9	M4	V_{SS}	AA35
P006	C9	P056	B28	P106	R33	P156	AN33	P206	AP16	P256	AG3	P306/RA0	G3	V_{SS}	AC1
P007	F10	P057	D24	P107	R31	P157	AJ31	P207	AM16	P257	AE7	P307/RA1	M6	V_{SS}	AE35
P008	D10	P058	C27	P108	T32	P158	AL29	P208	AR15	P258	AF4	P308/RA2	H4	V_{SS}	AJ35
P009	G11	P059	F24	P109	T30	P159	AJ29	P209	AK16	P259	AE5	P309/RA3	L5	V_{SS}	AL1
P010	B10	P060	C29	P110	T34	P160	AK28	P210	AN15	P260	AF2	P310/RA4	F2	V_{SS}	AR1
P011	E11	P061	E25	P111	U31	P161	AP34	P211	AL15	P261	AD6	P311/RA5	L7	V_{SS}	AR25
P012	C11	P062	D28	P112	U33	P162	AP30	P212	AP14	P262	AE3	P312/RA6	F4	V_{SS}	AR29
P013	F12	P063	G25	P113	U29	P163	AM32	P213	AJ15	P263	AC7	P313/RA7	E3	V_{SS}	AR33
P014	D12	P064	B30	P114	U35	P164	AN29	P214	AP12	P264	AD4	P314/RA8	D2	V_{SS}	AR5
P015	G13	P065	D26	P115	V32	P165	AP32	P215	AM14	P265	AC5	P315/RA9	E5	V_{SS}	AR9
P016	B12	P066	D30	P116	V34	P166	AJ27	P216	AN13	P266	AD2	P316/C0	F6	V_{SS}	B2
P017	E13	P067	F26	P117	V30	P167	AM30	P217	AK14	P267	AB6	P317/C1	C3	V_{SS}	J35
P018	C13	P068	C31	P118	W33	P168	AL27	P218	AP10	P268	AC3	P318/$\overline{WE}$	E7	V_{SS}	L1
P019	F14	P069	E27	P119	W31	P169	AN31	P219	AL13	P269	AB4	P319/$\overline{STROBE}$	G7	V_{SS}	N35
P020	B14	P070	B32	P120	W35	P170	AP28	P220	AN11	P270	AB2	RID	H6	V_{SS}	R1
P021	D14	P071	G27	P121	W29	P171	AM28	P221	AJ13	P271	AA7	ROD	J7	V_{SS}	A11
P022	C15	P072	E31	P122	Y34	P172	AN27	P222	AP8	P272	AA3	RPU	G5	V_{SS}	A23
P023	G15	P073	F28	P123	Y32	P173	AK26	P223	AM12	P273	AA5	TCK	C5	V_{SS}	A27
P024	A15	P074	F30	P124	AA33	P174	AM26	P224	AN9	P274	Y4	TDI	D4	V_{SS}	A3
P025	E15	P075	E29	P125	Y30	P175	AJ25	P225	AK12	P275	Y6	TDO	D6	V_{SS}	A31
P026	D16	P076	G29	P126	AB34	P176	AP26	P226	AN7	P276	Y2	TMS	B4	V_{SS}	A35
P027	F16	P077	B34	P127	AA31	P177	AL25	P227	AL11	P277	W5	TRST*	D8	V_{SS}	A7
P028	B16	P078	H30	P128	AD34	P178	AN25	P228	AM8	P278	W3	V_{DD}	A13	V_{SS}	AG1
P029	E17	P079	D32	P129	AA29	P179	AK24	P229	AJ11	P279	W7	V_{DD}	A25	V_{SS}	AN35
P030	C17	P080	F34	P130	AC33	P180	AM24	P230	AP6	P280	W1	V_{DD}	A29	V_{SS}	AR13
P031	G17	P081	D34	P131	AB32	P181	AJ23	P231	AM10	P281	V4	V_{DD}	A33	V_{SS}	C1
P032	A17	P082	G33	P132	AF34	P182	AP24	P232	AM6	P282	V2	V_{DD}	A5	V_{SS}	E35
P033	D18	P083	F32	P133	AB30	P183	AL23	P233	AK10	P283	V6	V_{DD}	A9	V_{SS}	G1
P034	B18	P084	J29	P134	AE33	P184	AN23	P234	AN5	P284	U3	V_{DD}	AA1		
P035	F18	P085	E33	P135	AC31	P185	AK22	P235	AL9	P285	U5	V_{DD}	AC35		
P036	C19	P086	J31	P136	AH34	P186	AP22	P236	AP4	P286	U1	V_{DD}	AE1		
P037	E19	P087	H32	P137	AC29	P187	AM22	P237	AJ9	P287	U7	V_{DD}	AG35		
P038	A19	P088	H34	P138	AG33	P188	AN21	P238	AL5	P288	T2	V_{DD}	AJ1		
P039	G19	P089	K30	P139	AD32	P189	AJ21	P239	AK8	P289	T4	V_{DD}	AL35		
P040	B20	P090	J33	P140	AJ33	P190	AR21	P240	AK6	P290	R3	V_{DD}	AN1		
P041	D20	P091	L29	P141	AD30	P191	AL21	P241	AL7	P291	T6	V_{DD}	AR11		
P042	A21	P092	K32	P142	AH32	P192	AM20	P242	AJ7	P292	P2	V_{DD}	AR23		

IQ320 [PPGA/391L] Package Pinout by Pin Location

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
A3	V_{SS}	C33	$\overline{OE0}$	F28	P073	M2	P294	W5	P277	AF6	P255	AK30	P154	AN25	P178
A5	V_{DD}	C35	V_{DD}	F30	P074	M4	P305/CA9	W7	P279	AF30	P149	AK32	P146	AN27	P172
A7	V_{SS}	D2	P314/RA8	F32	P083	M6	P307/RA1	W29	P121	AF32	P147	AK34	P144	AN29	P164
A9	V_{DD}	D4	TDI	F34	P080	M30	P095	W31	P119	AF34	P132	AL1	V_{SS}	AN31	P169
A11	V_{SS}	D6	TDO	G1	V_{SS}	M32	P098	W33	P118	AG1	V_{SS}	AL3	P251	AN33	P156
A13	V_{DD}	D8	TRST*	G3	P306/RA0	M34	P100	W35	P120	AG3	P256	AL5	P238	AN35	V_{SS}
A15	P024	D10	P008	G5	RPU	N1	V_{DD}	Y2	P276	AG5	P252	AL7	P241	AP2	P243
A17	P032	D12	P014	G7	P319/$\overline{STROBE}$	N3	P296/CA0	Y4	P274	AG7	P250	AL9	P235	AP4	P236
A19	P038	D14	P021	G9	P003	N5	P301/CA5	Y6	P275	AG29	P153	AL11	P227	AP6	P230
A21	P042	D16	P026	G11	P009	N7	P303/CA7	Y30	P125	AG31	P151	AL13	P219	AP8	P222
A23	V_{SS}	D18	P033	G13	P015	N29	P097	Y32	P123	AG33	P138	AL15	P211	AP10	P218
A25	V_{DD}	D20	P041	G15	P023	N31	P099	Y34	P122	AG35	V_{DD}	AL17	P203	AP12	P214
A27	V_{SS}	D22	P049	G17	P031	N33	P102	AA1	V_{DD}	AH2	P254	AL19	P195	AP14	P212
A29	V_{DD}	D24	P057	G19	P039	N35	V_{SS}	AA3	P272	AH4	P253	AL21	P191	AP16	P206
A31	V_{SS}	D26	P065	G21	P047	P2	P292	AA5	P273	AH6	P244	AL23	P183	AP18	P200
A33	V_{DD}	D28	P062	G23	P055	P4	P297/CA1	AA7	P271	AH30	P155	AL25	P177	AP20	P194
A35	V_{SS}	D30	P066	G25	P063	P6	P299/CA3	AA29	P129	AH32	P142	AL27	P168	AP22	P186
B2	V_{SS}	D32	P079	G27	P071	P30	P101	AA31	P127	AH34	P136	AL29	P158	AP24	P182
B4	TMS	D34	P081	G29	P076	P32	P103	AA33	P124	AJ1	V_{DD}	AL31	P152	AP26	P176
B6	P001	E1	V_{DD}	G31	$\overline{OE1}$	P34	P104	AA35	V_{SS}	AJ3	P248	AL33	P148	AP28	P170
B8	P005	E3	P313/RA7	G33	P082	R1	V_{SS}	AB2	P270	AJ5	$\overline{OE3}$	AL35	V_{DD}	AP30	P162
B10	P010	E5	P315/RA9	G35	V_{DD}	R3	P290	AB4	P269	AJ7	P242	AM2	P247	AP32	P165
B12	P016	E7	P318/$\overline{WE}$	H2	P302/CA6	R5	P293	AB6	P267	AJ9	P237	AM4	P245	AP34	P161
B14	P020	E9	P004	H4	P308/RA2	R7	P295	AB30	P133	AJ11	P229	AM6	P232	AR1	V_{SS}
B16	P028	E11	P011	H6	RID	R29	P105	AB32	P131	AJ13	P221	AM8	P228	AR3	V_{DD}
B18	P034	E13	P017	H30	P078	R31	P107	AB34	P126	AJ15	P213	AM10	P231	AR5	V_{SS}
B20	P040	E15	P025	H32	P087	R33	P106	AC1	V_{SS}	AJ17	P205	AM12	P223	AR7	V_{DD}
B22	P046	E17	P029	H34	P088	R35	V_{DD}	AC3	P268	AJ19	P197	AM14	P215	AR9	V_{SS}
B24	P048	E19	P037	J1	V_{DD}	T2	P288	AC5	P265	AJ21	P189	AM16	P207	AR11	V_{DD}
B26	P052	E21	P045	J3	P304/CA8	T4	P289	AC7	P263	AJ23	P181	AM18	P199	AR13	V_{SS}
B28	P056	E23	P053	J5	OCLK	T6	P291	AC29	P137	AJ25	P175	AM20	P192	AR15	P208
B30	P064	E25	P061	J7	ROD	T30	P109	AC31	P135	AJ27	P166	AM22	P187	AR17	P204
B32	P070	E27	P069	J29	P084	T32	P108	AC33	P130	AJ29	P159	AM24	P180	AR19	P198
B34	P077	E29	P075	J31	P086	T34	P110	AC35	V_{DD}	AJ31	P157	AM26	P174	AR21	P190
C1	V_{SS}	E31	P072	J33	P090	U1	P286	AD2	P266	AJ33	P140	AM28	P171	AR23	V_{DD}
C3	P317/C1	E33	P085	J35	V_{SS}	U3	P284	AD4	P264	AJ35	V_{SS}	AM30	P167	AR25	V_{SS}
C5	TCK	E35	V_{SS}	K2	P298/CA2	U5	P285	AD6	P261	AK2	P246	AM32	P163	AR27	V_{DD}
C7	P002	F2	P310/RA4	K4	NC	U7	P287	AD30	P141	AK4	P249	AM34	P150	AR29	V_{SS}
C9	P006	F4	P312/RA6	K6	ICLK	U29	P113	AD32	P139	AK6	P240	AN1	V_{DD}	AR31	V_{DD}
C11	P012	F6	P316/C0	K30	P089	U31	P111	AD34	P128	AK8	P239	AN3	$\overline{OE2}$	AR33	V_{SS}
C13	P018	F8	P000	K32	P092	U33	P112	AE1	V_{DD}	AK10	P233	AN5	P234	AR35	V_{DD}
C15	P022	F10	P007	K34	P094	U35	P114	AE3	P262	AK12	P225	AN7	P226		
C17	P030	F12	P013	L1	V_{SS}	V2	P282	AE5	P259	AK14	P217	AN9	P224		
C19	P036	F14	P019	L3	P300/CA4	V4	P281	AE7	P257	AK16	P209	AN11	P220		
C21	P044	F16	P027	L5	P309/RA3	V6	P283	AE29	P145	AK18	P201	AN13	P216		
C23	P050	F18	P035	L7	P311/RA5	V30	P117	AE31	P143	AK20	P193	AN15	P210		
C25	P054	F20	P043	L29	P091	V32	P115	AE33	P134	AK22	P185	AN17	P202		
C27	P058	F22	P051	L31	P093	V34	P116	AE35	V_{SS}	AK24	P179	AN19	P196		
C29	P060	F24	P059	L33	P096	W1	P280	AF2	P260	AK26	P173	AN21	P188		
C31	P068	F26	P067	L35	V_{DD}	W3	P278	AF4	P258	AK28	P160	AN23	P184		

IQ320 [PBGA/416L] Package Pinout by Name

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
NC	F3	P045	B18	P097	G27	P149	AA25	P201	AE15	P253	AC1	P305/CA9	G1	V_{DD}	N25
ICLK	E2	P046	C16	P098	K25	P150	Y23	P202	AB14	P254	X4	P306/RA0	K4	V_{DD}	P1
OCLK	D1	P047	C18	P099	H25	P151	AC27	P203	AE14	P255	AB2	P307/RA1	G2	V_{DD}	P26
$\overline{OE0}$	D22	P048	D16	P100	L23	P152	U23	P204	AC14	P256	W5	P308/RA2	K5	V_{DD}	P27
$\overline{OE1}$	E24	P049	B19	P101	H26	P153	AB25	P205	AE13	P257	AA3	P309/RA3	G3	V_{DD}	R2
$\overline{OE2}$	AB5	P050	E16	P102	L24	P154	AA24	P206	AD13	P258	W4	P310/RA4	J4	V_{DD}	R3
$\overline{OE3}$	AA5	P051	C19	P103	J25	P155	AC26	P207	AE12	P259	AA2	P311/RA5	F2	V_{DD}	V1
P000	D5	P052	C17	P104	L25	P156	AA23	P208	AC13	P260	V5	P312/RA6	J5	V_{DD}	W2
P001	E14	P053	B20	P105	J26	P157	AD25	P209	AE11	P261	Y3	P313/RA7	H5	V_{DD}	W27
P002	E6	P054	D17	P106	M25	P158	AB23	P210	AB13	P262	V4	P314/RA8	G4	V_{DD}	X1
P003	E11	P055	C20	P107	J27	P159	AC25	P211	AF10	P263	Y2	P315/RA9	G5	V_{DD}	X24
P004	D6	P056	E17	P108	M23	P160	AB22	P212	AC12	P264	V3	P316/C0	F4	V_{SS}	A6
P005	E9	P057	A21	P109	K26	P161	AD24	P213	AE10	P265	Y1	P317/C1	F5	V_{SS}	A11
P006	E8	P058	D18	P110	M24	P162	AC23	P214	AB12	P266	U5	P318/$\overline{WE}$	E5	V_{SS}	A12
P007	C6	P059	B21	P111	L26	P163	AE25	P215	AD10	P267	X3	P319/$\overline{STROBE}$	D3	V_{SS}	A16
P008	E7	P060	D19	P112	N23	P164	AB21	P216	AC11	P268	U4	RID	D2	V_{SS}	A17
P009	B6	P061	C21	P113	M26	P165	AE24	P217	AE9	P269	X2	ROD	E3	V_{SS}	A20
P010	D7	P062	E18	P114	N24	P166	AC22	P218	AC10	P270	U3	RPU	C3	V_{SS}	A22
P011	C7	P063	B22	P115	N27	P167	AD23	P219	AD9	P271	W3	TCK	A4	V_{SS}	AA1
P012	E10	P064	E19	P116	P25	P168	AC21	P220	AC9	P272	T5	TDI	B3	V_{SS}	AA27
P013	B7	P065	C22	P117	N26	P169	AF24	P221	AE8	P273	W1	TDO	C5	V_{SS}	AB24
P014	D9	P066	D20	P118	P23	P170	AB20	P222	AB11	P274	T4	TMS	B4	V_{SS}	AB26
P015	A7	P067	B23	P119	R26	P171	AE23	P223	AD8	P275	V2	TRST*	B5	V_{SS}	AC4
P016	D8	P068	E20	P120	P24	P172	AC20	P224	AC8	P276	T3	V_{DD}	A5	V_{SS}	AC24
P017	C8	P069	A24	P121	R27	P173	AD22	P225	AF7	P277	U2	V_{DD}	A8	V_{SS}	AD26
P018	D10	P070	D21	P122	R25	P174	AB19	P226	AB10	P278	R4	V_{DD}	A10	V_{SS}	AE3
P019	B8	P071	C23	P123	T26	P175	AE22	P227	AE7	P279	T2	V_{DD}	A14	V_{SS}	AF6
P020	C10	P072	E21	P124	R24	P176	AC19	P228	AB8	P280	R5	V_{DD}	A19	V_{SS}	AF8
P021	C9	P073	B24	P125	U26	P177	AD21	P229	AD7	P281	R1	V_{DD}	A23	V_{SS}	AF11
P022	D11	P074	E22	P126	R23	P178	AB18	P230	AB9	P282	P3	V_{DD}	AB1	V_{SS}	AF12
P023	B9	P075	C25	P127	V27	P179	AE21	P231	AE6	P283	P2	V_{DD}	AB27	V_{SS}	AF16
P024	C11	P076	C24	P128	T25	P180	AC18	P232	AB7	P284	P4	V_{DD}	AD11	V_{SS}	AF17
P025	A9	P077	D25	P129	V26	P181	AF21	P233	AD6	P285	N1	V_{DD}	AD12	V_{SS}	AF22
P026	E12	P078	E23	P130	T24	P182	AD18	P234	AC7	P286	N3	V_{DD}	AD15	V_{SS}	B25
P027	B10	P079	C26	P131	V25	P183	AD20	P235	AE5	P287	M2	V_{DD}	AF5	V_{SS}	C2
P028	D12	P080	F24	P132	T23	P184	AB17	P236	AC6	P288	P5	V_{DD}	AF9	V_{SS}	C4
P029	B11	P081	D26	P133	W26	P185	AE20	P237	AF4	P289	L2	V_{DD}	AF13	V_{SS}	D4
P030	C12	P082	G23	P134	U25	P186	AC17	P238	AB6	P290	N4	V_{DD}	AF14	V_{SS}	D23
P031	B12	P083	E25	P135	W25	P187	AD19	P239	AD5	P291	K1	V_{DD}	AF18	V_{SS}	D24
P032	E13	P084	G24	P136	U24	P188	AD17	P240	AC5	P292	M3	V_{DD}	AF20	V_{SS}	E4
P033	A13	P085	D27	P137	X26	P189	AE19	P241	AE4	P293	K2	V_{DD}	AF23	V_{SS}	F1
P034	D13	P086	H23	P138	V24	P190	AB16	P242	AD3	P294	L3	V_{DD}	B13	V_{SS}	F27
P035	B14	P087	E26	P139	X25	P191	AF19	P243	AD4	P295	K3	V_{DD}	B15	V_{SS}	H1
P036	C14	P088	H24	P140	W24	P192	AC16	P244	AB4	P296/CA0	N5	V_{DD}	C13	V_{SS}	L1
P037	A15	P089	F25	P141	Y27	P193	AE18	P245	AC3	P297/CA1	J2	V_{DD}	E1	V_{SS}	L27
P038	D14	P090	J23	P142	V23	P194	AD16	P246	AA4	P298/CA2	M5	V_{DD}	E27	V_{SS}	M1
P039	B16	P091	F26	P143	Y26	P195	AE17	P247	AD2	P299/CA3	J3	V_{DD}	F23	V_{SS}	M27
P040	C15	P092	J24	P144	Y24	P196	AC15	P248	Y5	P300/CA4	M4	V_{DD}	H27	V_{SS}	T1
P041	B17	P093	G25	P145	Y25	P197	AE16	P249	AC2	P301/CA5	H2	V_{DD}	H4	V_{SS}	T27
P042	D15	P094	K23	P146	X23	P198	AB15	P250	Y4	P302/CA6	L4	V_{DD}	J1	V_{SS}	U1
P043	A18	P095	G26	P147	AA26	P199	AF15	P251	AB3	P303/CA7	H3	V_{DD}	K27	V_{SS}	U27
P044	E15	P096	K24	P148	W23	P200	AD14	P252	X5	P304/CA8	L5	V_{DD}	N2	V_{SS}	X27

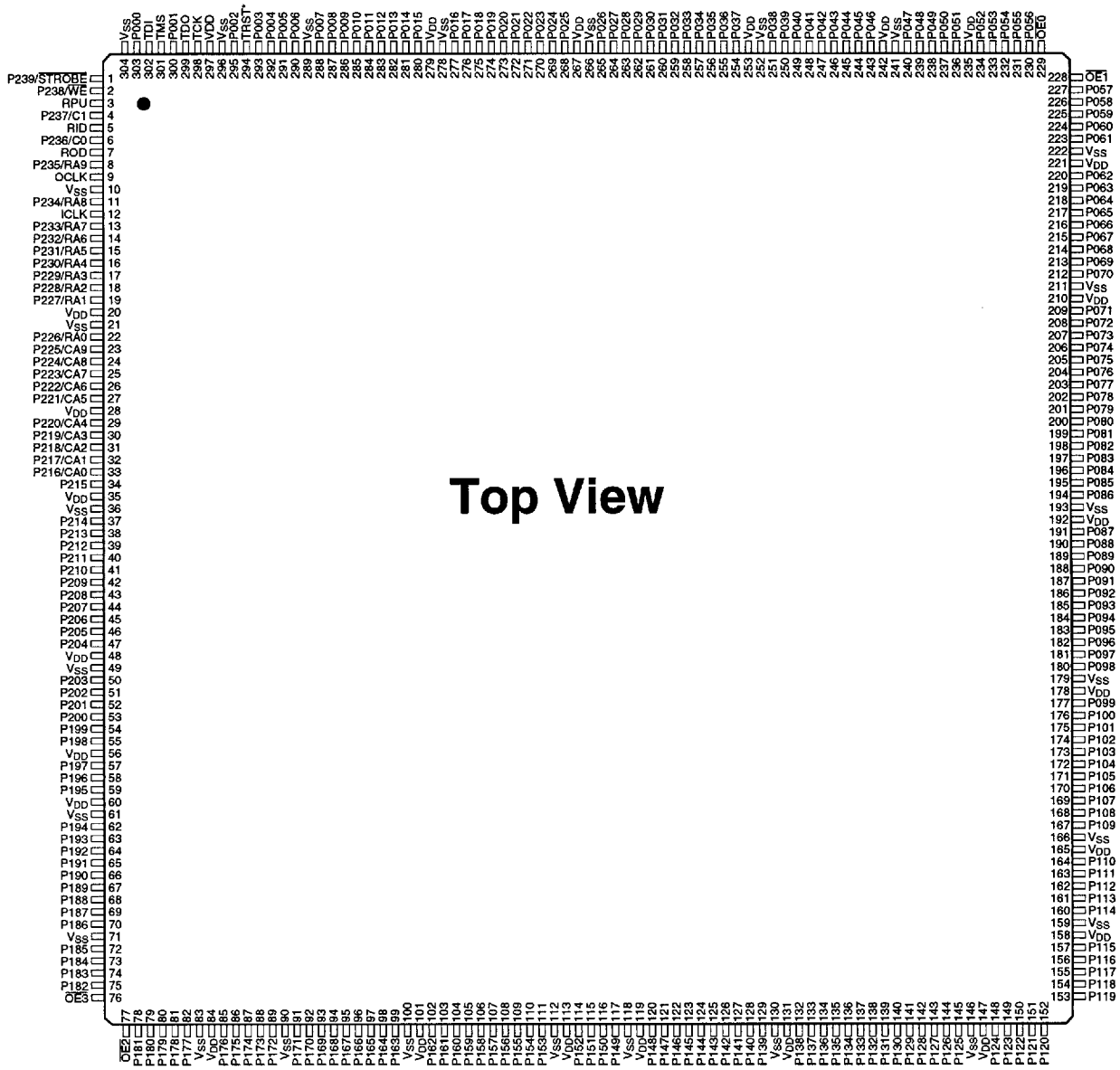
IQ320 [PBGA/416L] Package Pinout by Pin Location

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
A4	TCK	C11	P024	E11	P003	J24	P092	P27	V_{DD}	X3	P267	AB26	VSS	AD26	V_{SS}
A5	V_{DD}	C12	P030	E12	P026	J25	P103	R1	P281	X4	P254	AB27	V_{DD}	AE3	V_{SS}
A6	V_{SS}	C13	V_{DD}	E13	P032	J26	P105	R2	V_{DD}	X5	P252	AC1	P253	AE4	P241
A7	P015	C14	P036	E14	P001	J27	P107	R3	V_{DD}	X23	P146	AC2	P249	AE5	P235
A8	V_{DD}	C15	P040	E15	P044	K1	P291	R4	P278	X24	V_{DD}	AC3	P245	AE6	P231
A9	P025	C16	P046	E16	P050	K2	P293	R5	P280	X25	P139	AC4	V_{SS}	AE7	P227
A10	V_{DD}	C17	P052	E17	P056	K3	P295	R23	P126	X26	P137	AC5	P240	AE8	P221
A11	V_{SS}	C18	P047	E18	P062	K4	P306/RA0	R24	P124	X27	V_{SS}	AC6	P236	AE9	P217
A12	V_{SS}	C19	P051	E19	P064	K5	P308/RA2	R25	P122	Y1	P265	AC7	P234	AE10	P213
A13	P033	C20	P055	E20	P068	K23	P094	R26	P119	Y2	P263	AC8	P224	AE11	P209
A14	V_{DD}	C21	P061	E21	P072	K24	P096	R27	P121	Y3	P261	AC9	P220	AE12	P207
A15	P037	C22	P065	E22	P074	K25	P098	T1	V_{SS}	Y4	P250	AC10	P218	AE13	P205
A16	V_{SS}	C23	P071	E23	P078	K26	P109	T2	P279	Y5	P248	AC11	P216	AE14	P203
A17	V_{SS}	C24	P076	E24	$\overline{OE1}$	K27	V_{DD}	T3	P276	Y23	P150	AC12	P212	AE15	P201
A18	P043	C25	P075	E25	P083	L1	V_{SS}	T4	P274	Y24	P144	AC13	P208	AE16	P197
A19	V_{DD}	C26	P079	E26	P087	L2	P289	T5	P272	Y25	P145	AC14	P204	AE17	P195
A20	V_{SS}	D1	OCLK	E27	V_{DD}	L3	P294	T23	P132	Y26	P143	AC15	P196	AE18	P193
A21	P057	D2	RID	F1	V_{SS}	L4	P302/CA6	T24	P130	Y27	P141	AC16	P192	AE19	P189
A22	V_{SS}	D3	P319/$\overline{STROBE}$	F2	P311/RA5	L5	P304/CA8	T25	P128	AA1	V_{SS}	AC17	P186	AE20	P185
A23	V_{DD}	D4	V_{SS}	F3	NC	L23	P100	T26	P123	AA2	P259	AC18	P180	AE21	P179
A24	P069	D5	P000	F4	P316/C0	L24	P102	T27	V_{SS}	AA3	P257	AC19	P176	AE22	P175
B3	TDI	D6	P004	F5	P317/C1	L25	P104	U1	V_{SS}	AA4	P246	AC20	P172	AE23	P171
B4	TMS	D7	P010	F23	V_{DD}	L26	P111	U2	P277	AA5	$\overline{OE3}$	AC21	P168	AE24	P165
B5	TRST*	D8	P016	F24	P080	L27	V_{SS}	U3	P270	AA23	P156	AC22	P166	AE25	P163
B6	P009	D9	P014	F25	P089	M1	V_{SS}	U4	P268	AA24	P154	AC23	P162	AF4	P237
B7	P013	D10	P018	F26	P091	M2	P287	U5	P266	AA25	P149	AC24	V_{SS}	AF5	V_{DD}
B8	P019	D11	P022	F27	V_{SS}	M3	P292	U23	P152	AA26	P147	AC25	P159	AF6	V_{SS}
B9	P023	D12	P028	G1	P305/CA9	M4	P300/CA4	U24	P136	AA27	V_{SS}	AC26	P155	AF7	P225
B10	P027	D13	P034	G2	P307/RA1	M5	P298/CA2	U25	P134	AB1	V_{DD}	AC27	P151	AF8	V_{SS}
B11	P029	D14	P038	G3	P309/RA3	M23	P108	U26	P125	AB2	P255	AD2	P247	AF9	V_{DD}
B12	P031	D15	P042	G4	P314/RA8	M24	P110	U27	V_{SS}	AB3	P251	AD3	P242	AF10	P211
B13	V_{DD}	D16	P048	G5	P315/RA9	M25	P106	V1	V_{DD}	AB4	P244	AD4	P243	AF11	V_{SS}
B14	P035	D17	P054	G23	P082	M26	P113	V2	P275	AB5	$\overline{OE2}$	AD5	P239	AF12	V_{SS}
B15	V_{DD}	D18	P058	G24	P084	M27	V_{SS}	V3	P264	AB6	P238	AD6	P233	AF13	V_{DD}
B16	P039	D19	P060	G25	P093	N1	P285	V4	P262	AB7	P232	AD7	P229	AF14	V_{DD}
B17	P041	D20	P066	G26	P095	N2	V_{DD}	V5	P260	AB8	P228	AD8	P223	AF15	P199
B18	P045	D21	P070	G27	P097	N3	P286	V23	P142	AB9	P230	AD9	P219	AF16	V_{SS}
B19	P049	D22	$\overline{OE0}$	H1	V_{SS}	N4	P290	V24	P138	AB10	P226	AD10	P215	AF17	V_{SS}
B20	P053	D23	V_{SS}	H2	P301/CA5	N5	P296/CA0	V25	P131	AB11	P222	AD11	V_{DD}	AF18	V_{DD}
B21	P059	D24	V_{SS}	H3	P303/CA7	N23	P112	V26	P129	AB12	P214	AD12	V_{DD}	AF19	P191
B22	P063	D25	P077	H4	V_{DD}	N24	P114	V27	P127	AB13	P210	AD13	P206	AF20	V_{DD}
B23	P067	D26	P081	H5	P313/RA7	N25	V_{DD}	W1	P273	AB14	P202	AD14	P200	AF21	P181
B24	P073	D27	P085	H23	P086	N26	P117	W2	V_{DD}	AB15	P198	AD15	V_{DD}	AF22	V_{SS}
B25	V_{SS}	E1	V_{DD}	H24	P088	N27	P115	W3	P271	AB16	P190	AD16	P194	AF23	V_{DD}
C2	V_{SS}	E2	ICLK	H25	P099	P1	V_{DD}	W4	P258	AB17	P184	AD17	P188	AF24	P169
C3	RPU	E3	ROD	H26	P101	P2	P283	W5	P256	AB18	P178	AD18	P182		
C4	V_{SS}	E4	V_{SS}	H27	V_{DD}	P3	P282	W23	P148	AB19	P174	AD19	P187		
C5	TDO	E5	P318/$\overline{WE}$	J1	V_{DD}	P4	P284	W24	P140	AB20	P170	AD20	P183		
C6	P007	E6	P002	J2	P297/CA1	P5	P288	W25	P135	AB21	P164	AD21	P177		
C7	P011	E7	P008	J3	P299/CA3	P23	P118	W26	P133	AB22	P160	AD22	P173		
C8	P017	E8	P006	J4	P310/RA4	P24	P120	W27	V_{DD}	AB23	P158	AD23	P167		
C9	P021	E9	P005	J5	P312/RA6	P25	P116	X1	V_{DD}	AB24	V_{SS}	AD24	P161		
C10	P020	E10	P012	J23	P090	P26	V_{DD}	X2	P269	AB25	P153	AD25	P157		

IQ240B [MQUAD®/304L] Package Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P239/STROBE	39	P212	77	$\overline{OE2}$	115	P151	153	P119	191	P087	229	$\overline{OE0}$	267	V_{DD}
2	P238/$\overline{WE}$	40	P211	78	P181	116	P150	154	P118	192	V_{DD}	230	P056	268	P025
3	RPU	41	P210	79	P180	117	P149	155	P117	193	V_{SS}	231	P055	269	P024
4	P237/C1	42	P209	80	P179	118	V_{SS}	156	P116	194	P086	232	P054	270	P023
5	RID	43	P208	81	P178	119	V_{DD}	157	P115	195	P085	233	P053	271	P022
6	P236/C0	44	P207	82	P177	120	P148	158	V_{DD}	196	P084	234	P052	272	P021
7	ROD	45	P206	83	V_{SS}	121	P147	159	V_{SS}	197	P083	235	V_{DD}	273	P020
8	P235/RA9	46	P205	84	V_{DD}	122	P146	160	P114	198	P082	236	P051	274	P019
9	OCLK	47	P204	85	P176	123	P145	161	P113	199	P081	237	P050	275	P018
10	V_{SS}	48	V_{DD}	86	P175	124	P144	162	P112	200	P080	238	P049	276	P017
11	P234/RA8	49	V_{SS}	87	P174	125	P143	163	P111	201	P079	239	P048	277	P016
12	ICLK	50	P203	88	P173	126	P142	164	P110	202	P078	240	P047	278	V_{SS}
13	P233/RA7	51	P202	89	P172	127	P141	165	V_{DD}	203	P077	241	V_{SS}	279	V_{DD}
14	P232/RA6	52	P201	90	V_{SS}	128	P140	166	V_{SS}	204	P076	242	V_{DD}	280	P015
15	P231/RA5	53	P200	91	P171	129	P139	167	P109	205	P075	243	P046	281	P014
16	P230/RA4	54	P199	92	P170	130	V_{SS}	168	P108	206	P074	244	P045	282	P013
17	P229/RA3	55	P198	93	P169	131	V_{DD}	169	P107	207	P073	245	P044	283	P012
18	P228/RA2	56	V_{DD}	94	P168	132	P138	170	P106	208	P072	246	P043	284	P011
19	P227/RA1	57	P197	95	P167	133	P137	171	P105	209	P071	247	P042	285	P010
20	V_{DD}	58	P196	96	P166	134	P136	172	P104	210	V_{DD}	248	P041	286	P009
21	V_{SS}	59	P195	97	P165	135	P135	173	P103	211	V_{SS}	249	P040	287	P008
22	P226/RA0	60	V_{DD}	98	P164	136	P134	174	P102	212	P070	250	P039	288	P007
23	P225/CA9	61	V_{SS}	99	P163	137	P133	175	P101	213	P069	251	P038	289	V_{SS}
24	P224/CA8	62	P194	100	V_{SS}	138	P132	176	P100	214	P068	252	V_{SS}	290	P006
25	P223/CA7	63	P193	101	V_{DD}	139	P131	177	P099	215	P067	253	V_{DD}	291	P005
26	P222/CA6	64	P192	102	P162	140	P130	178	V_{DD}	216	P066	254	P037	292	P004
27	P221/CA5	65	P191	103	P161	141	P129	179	V_{SS}	217	P065	255	P036	293	P003
28	V_{DD}	66	P190	104	P160	142	P128	180	P098	218	P064	256	P035	294	TRST*
29	P220/CA4	67	P189	105	P159	143	P127	181	P097	219	P063	257	P034	295	P002
30	P219/CA3	68	P188	106	P158	144	P126	182	P096	220	P062	258	P033	296	V_{SS}
31	P218/CA2	69	P187	107	P157	145	P125	183	P095	221	V_{DD}	259	P032	297	V_{DD}
32	P217/CA1	70	P186	108	P156	146	V_{SS}	184	P094	222	V_{SS}	260	P031	298	TCK
33	P216/CA0	71	V_{SS}	109	P155	147	V_{DD}	185	P093	223	P061	261	P030	299	TDO
34	P215	72	P185	110	P154	148	P124	186	P092	224	P060	262	P029	300	P001
35	V_{DD}	73	P184	111	P153	149	P123	187	P091	225	P059	263	P028	301	TMS
36	V_{SS}	74	P183	112	V_{SS}	150	P122	188	P090	226	P058	264	P027	302	TDI
37	P214	75	P182	113	V_{DD}	151	P121	189	P089	227	P057	265	P026	303	P000
38	P213	76	$\overline{OE3}$	114	P152	152	P120	190	P088	228	$\overline{OE1}$	266	V_{SS}	304	V_{SS}

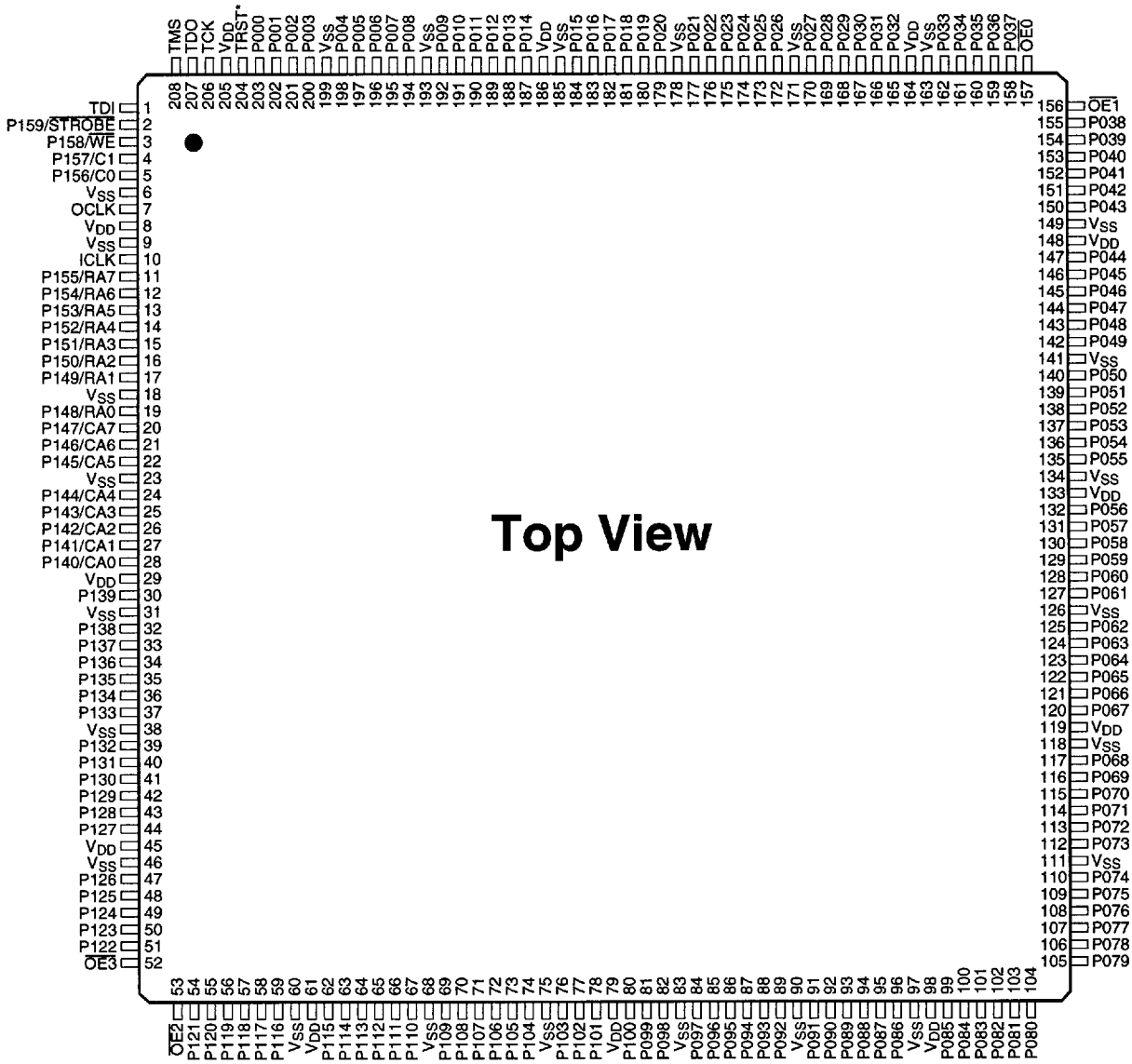
IQ240B [MQUAD®/304L] Package Pinout



IQ160 [MQUAD® and PQFP/208L] Package Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TDI	53	$\overline{OE2}$	105	P079	157	$\overline{OE0}$
2	P159/$\overline{STROBE}$	54	P121	106	P078	158	P037
3	P158/$\overline{WE}$	55	P120	107	P077	159	P036
4	P157/C1	56	P119	108	P076	160	P035
5	P156/C0	57	P118	109	P075	161	P034
6	V_{SS}	58	P117	110	P074	162	P033
7	OCLK	59	P116	111	V_{SS}	163	V_{SS}
8	V_{DD}	60	V_{SS}	112	P073	164	V_{DD}
9	V_{SS}	61	V_{DD}	113	P072	165	P032
10	ICLK	62	P115	114	P071	166	P031
11	P155/RA7	63	P114	115	P070	167	P030
12	P154/RA6	64	P113	116	P069	168	P029
13	P153/RA5	65	P112	117	P068	169	P028
14	P152/RA4	66	P111	118	V_{SS}	170	P027
15	P151/RA3	67	P110	119	V_{DD}	171	V_{SS}
16	P150/RA2	68	V_{SS}	120	P067	172	P026
17	P149/RA1	69	P109	121	P066	173	P025
18	V_{SS}	70	P108	122	P065	174	P024
19	P148/RA0	71	P107	123	P064	175	P023
20	P147/CA7	72	P106	124	P063	176	P022
21	P146/CA6	73	P105	125	P062	177	P021
22	P145/CA5	74	P104	126	V_{SS}	178	V_{SS}
23	V_{SS}	75	VSS	127	P061	179	P020
24	P144/CA4	76	P103	128	P060	180	P019
25	P143/CA3	77	P102	129	P059	181	P018
26	P142/CA2	78	P101	130	P058	182	P017
27	P141/CA1	79	V_{DD}	131	P057	183	P016
28	P140/CA0	80	P100	132	P056	184	P015
29	V_{DD}	81	P099	133	V_{DD}	185	V_{SS}
30	P139	82	P098	134	V_{SS}	186	V_{DD}
31	V_{SS}	83	V_{SS}	135	P055	187	P014
32	P138	84	P097	136	P054	188	P013
33	P137	85	P096	137	P053	189	P012
34	P136	86	P095	138	P052	190	P011
35	P135	87	P094	139	P051	191	P010
36	P134	88	P093	140	P050	192	P009
37	P133	89	P092	141	V_{SS}	193	V_{SS}
38	V_{SS}	90	V_{SS}	142	P049	194	P008
39	P132	91	P091	143	P048	195	P007
40	P131	92	P090	144	P047	196	P006
41	P130	93	P089	145	P046	197	P005
42	P129	94	P088	146	P045	198	P004
43	P128	95	P087	147	P044	199	V_{SS}
44	P127	96	P086	148	V_{DD}	200	P003
45	V_{DD}	97	V_{SS}	149	V_{SS}	201	P002
46	V_{SS}	98	V_{DD}	150	P043	202	P001
47	P126	99	P085	151	P042	203	P000
48	P125	100	P084	152	P041	204	TRST*
49	P124	101	P083	153	P040	205	V_{DD}
50	P123	102	P082	154	P039	206	TCK
51	P122	103	P081	155	P038	207	TDO
52	$\overline{OE3}$	104	P080	156	$\overline{OE1}$	208	TMS

IQ160 [MQUAD® and PQFP/208L] Package Pinout

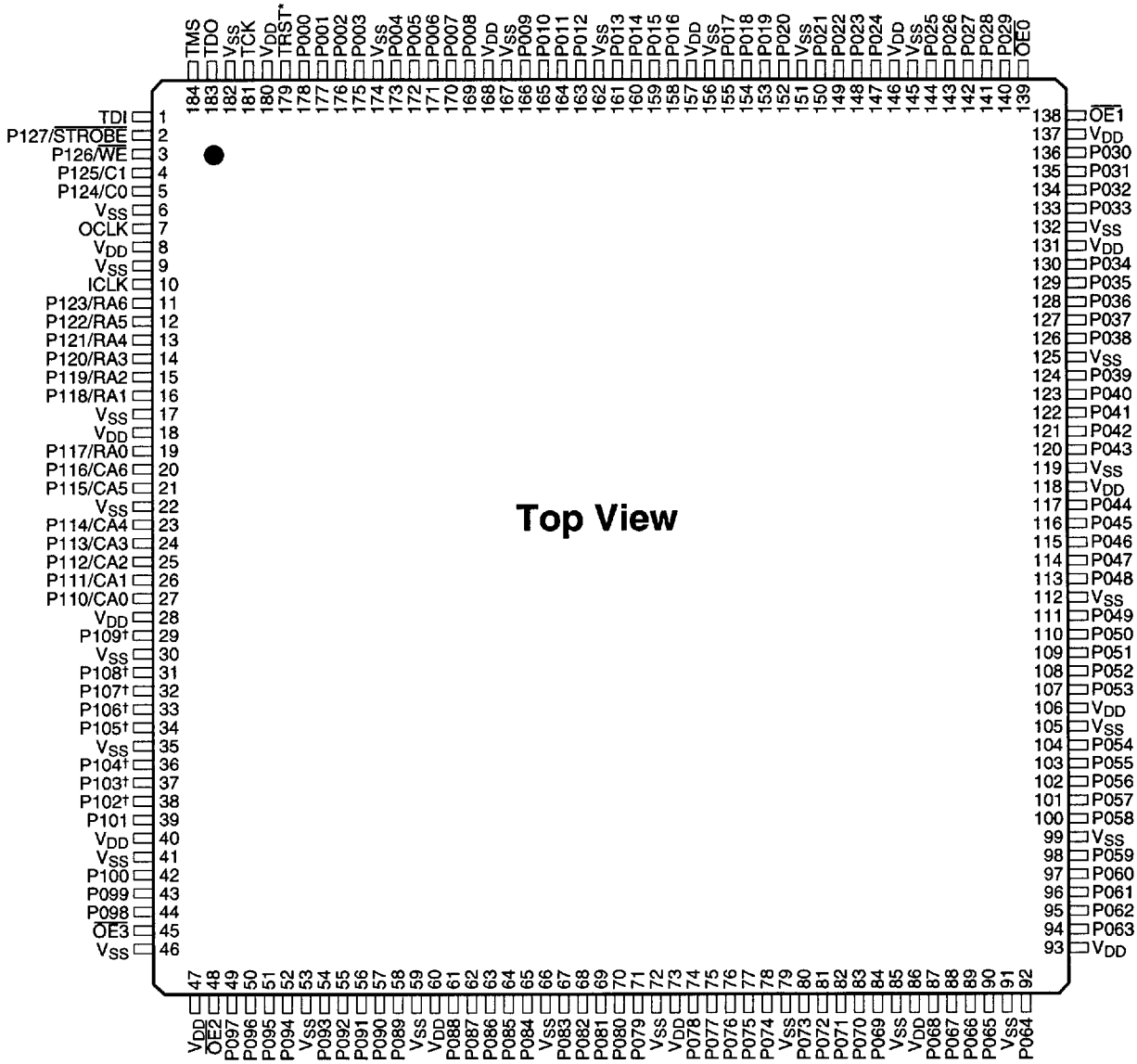


IQ128B [MQUAD® and PQFP/184L] Package Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TDI	47	V_{DD}	93	V_{DD}	139	$\overline{OE0}$
2	P127/$\overline{STROBE}$	48	$\overline{OE2}$	94	P063	140	P029
3	P126/$\overline{WE}$	49	P097	95	P062	141	P028
4	P125/C1	50	P096	96	P061	142	P027
5	P124/C0	51	P095	97	P060	143	P026
6	V_{SS}	52	P094	98	P059	144	P025
7	OCLK	53	V_{SS}	99	V_{SS}	145	V_{SS}
8	V_{DD}	54	P093	100	P058	146	V_{DD}
9	V_{SS}	55	P092	101	P057	147	P024
10	ICLK	56	P091	102	P056	148	P023
11	P123/RA6	57	P090	103	P055	149	P022
12	P122/RA5	58	P089	104	P054	150	P021
13	P121/RA4	59	V_{SS}	105	V_{SS}	151	V_{SS}
14	P120/RA3	60	V_{DD}	106	V_{DD}	152	P020
15	P119/RA2	61	P088	107	P053	153	P019
16	P118/RA1	62	P087	108	P052	154	P018
17	V_{SS}	63	P086	109	P051	155	P017
18	V_{DD}	64	P085	110	P050	156	V_{SS}
19	P117/RA0	65	P084	111	P049	157	V_{DD}
20	P116/CA6	66	V_{SS}	112	V_{SS}	158	P016
21	P115/CA5	67	P083	113	P048	159	P015
22	V_{SS}	68	P082	114	P047	160	P014
23	P114/CA4	69	P081	115	P046	161	P013
24	P113/CA3	70	P080	116	P045	162	V_{SS}
25	P112/CA2	71	P079	117	P044	163	P012
26	P111/CA1	72	V_{SS}	118	V_{DD}	164	P011
27	P110/CA0	73	V_{DD}	119	V_{SS}	165	P010
28	V_{DD}	74	P078	120	P043	166	P009
29	P109†	75	P077	121	P042	167	V_{SS}
30	V_{SS}	76	P076	122	P041	168	V_{DD}
31	P108†	77	P075	123	P040	169	P008
32	P107†	78	P074	124	P039	170	P007
33	P106†	79	V_{SS}	125	V_{SS}	171	P006
34	P105†	80	P073	126	P038	172	P005
35	V_{SS}	81	P072	127	P037	173	P004
36	P104†	82	P071	128	P036	174	V_{SS}
37	P103†	83	P070	129	P035	175	P003
38	P102†	84	P069	130	P034	176	P002
39	P101	85	V_{SS}	131	V_{DD}	177	P001
40	V_{DD}	86	V_{DD}	132	V_{SS}	178	P000
41	V_{SS}	87	P068	133	P033	179	TRST*
42	P100	88	P067	134	P032	180	V_{DD}
43	P099	89	P066	135	P031	181	TCK
44	P098	90	P065	136	P030	182	V_{SS}
45	$\overline{OE3}$	91	V_{SS}	137	V_{DD}	183	TDO
46	V_{SS}	92	P064	138	$\overline{OE1}$	184	TMS

† These I/O Ports cannot be addressed in RapidConnect Mode.

IQ128B [MQUAD® and PQFP/184L] Package Pinout

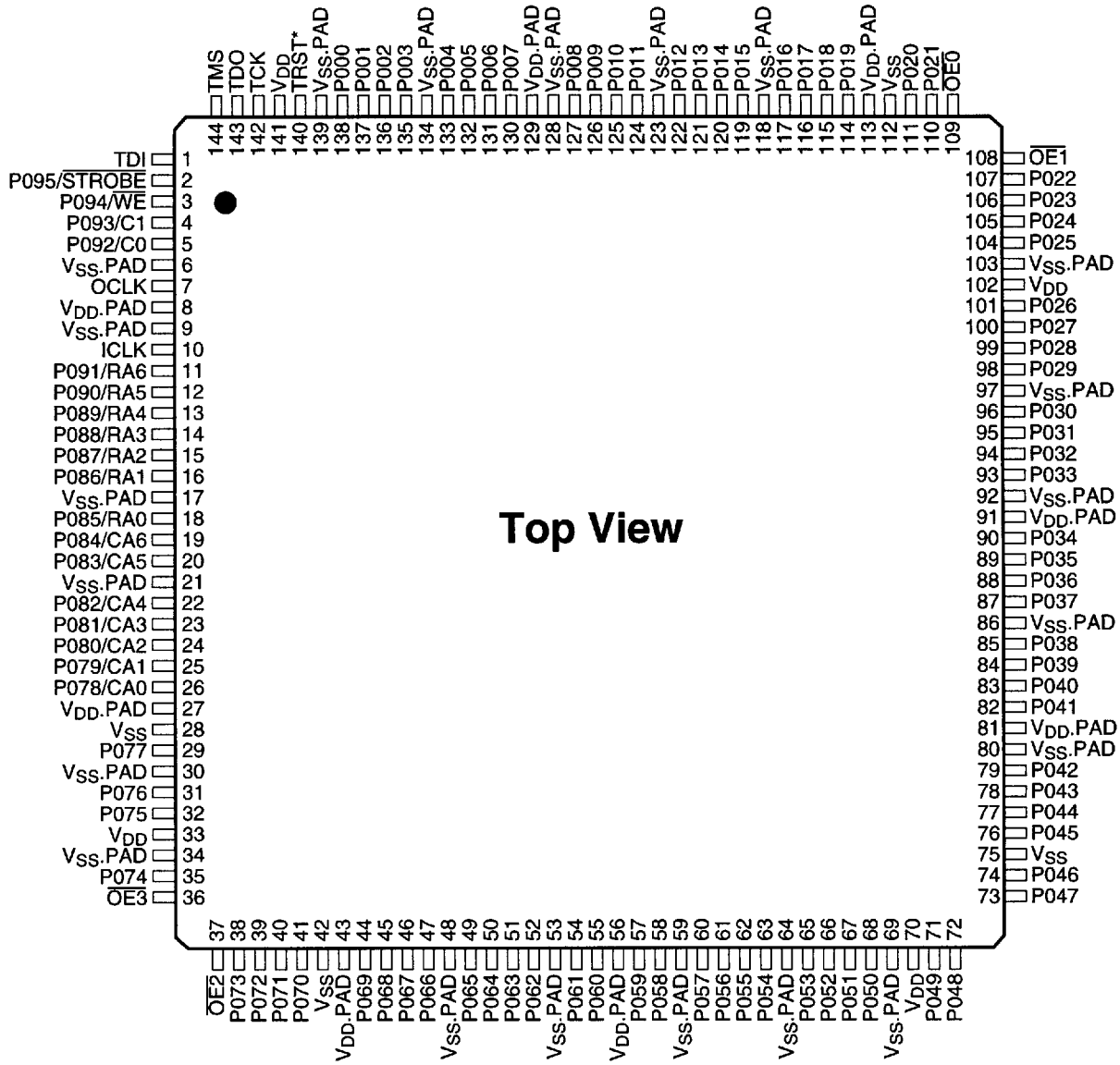


† These I/O Ports cannot be addressed in RapidConnect Mode.

IQ96 [MQUAD®, TQFP and PQFP/144L Package] Pinout

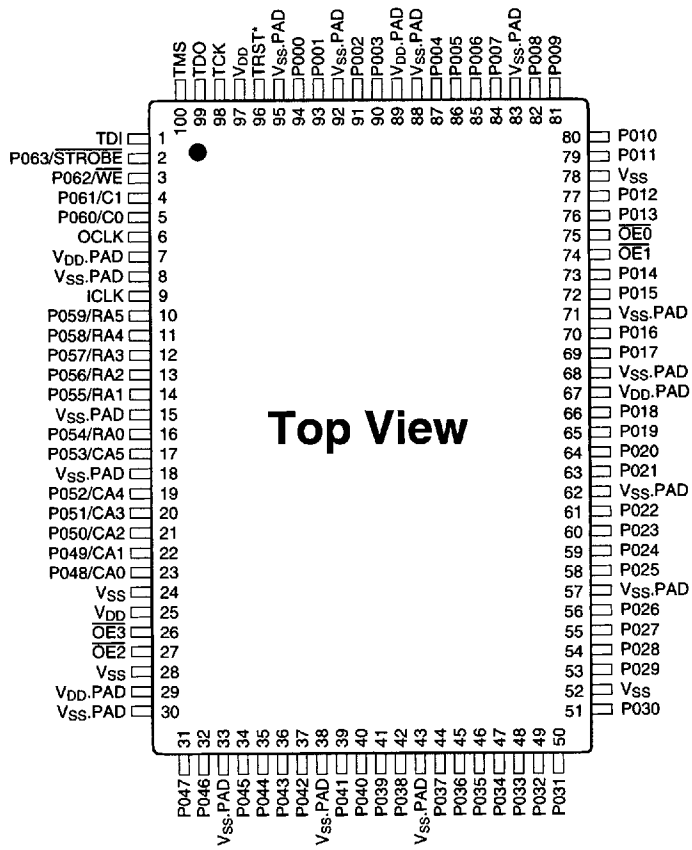
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TDI	37	$\overline{OE2}$	73	P047	109	$\overline{OE0}$
2	P095/$\overline{STROBE}$	38	P073	74	P046	110	P021
3	P094/$\overline{WE}$	39	P072	75	V_{SS}	111	P020
4	P093/C1	40	P071	76	P045	112	V_{SS}
5	P092/C0	41	P070	77	P044	113	V_{DD}.PAD
6	V_{SS}.PAD	42	V_{SS}	78	P043	114	P019
7	OCLK	43	V_{DD}.PAD	79	P042	115	P018
8	V_{DD}.PAD	44	P069	80	V_{SS}.PAD	116	P017
9	V_{SS}.PAD	45	P068	81	V_{DD}.PAD	117	P016
10	ICLK	46	P067	82	P041	118	V_{SS}.PAD
11	P091/RA6	47	P066	83	P040	119	P015
12	P090/RA5	48	V_{SS}.PAD	84	P039	120	P014
13	P089/RA4	49	P065	85	P038	121	P013
14	P088/RA3	50	P064	86	V_{SS}.PAD	122	P012
15	P087/RA2	51	P063	87	P037	123	V_{SS}.PAD
16	P086/RA1	52	P062	88	P036	124	P011
17	V_{SS}.PAD	53	V_{SS}.PAD	89	P035	125	P010
18	P085/RA0	54	P061	90	P034	126	P009
19	P084/CA6	55	P060	91	V_{DD}.PAD	127	P008
20	P083/CA5	56	V_{DD}.PAD	92	V_{SS}.PAD	128	V_{SS}.PAD
21	V_{SS}.PAD	57	P059	93	P033	129	V_{DD}.PAD
22	P082/CA4	58	P058	94	P032	130	P007
23	P081/CA3	59	V_{SS}.PAD	95	P031	131	P006
24	P080/CA2	60	P057	96	P030	132	P005
25	P079/CA1	61	P056	97	V_{SS}.PAD	133	P004
26	P078/CA0	62	P055	98	P029	134	V_{SS}.PAD
27	V_{DD}.PAD	63	P054	99	P028	135	P003
28	V_{SS}	64	V_{SS}.PAD	100	P027	136	P002
29	P077	65	P053	101	P026	137	P001
30	V_{SS}.PAD	66	P052	102	V_{DD}	138	P000
31	P076	67	P051	103	V_{SS}.PAD	139	V_{SS}.PAD
32	P075	68	P050	104	P025	140	TRST*
33	V_{DD}	69	V_{SS}.PAD	105	P024	141	V_{DD}
34	V_{SS}.PAD	70	V_{DD}	106	P023	142	TCK
35	P074	71	P049	107	P022	143	TDO
36	$\overline{OE3}$	72	P048	108	$\overline{OE1}$	144	TMS

IQ96 [MQUAD®, TQFP and PQFP/144L Package] Pinout



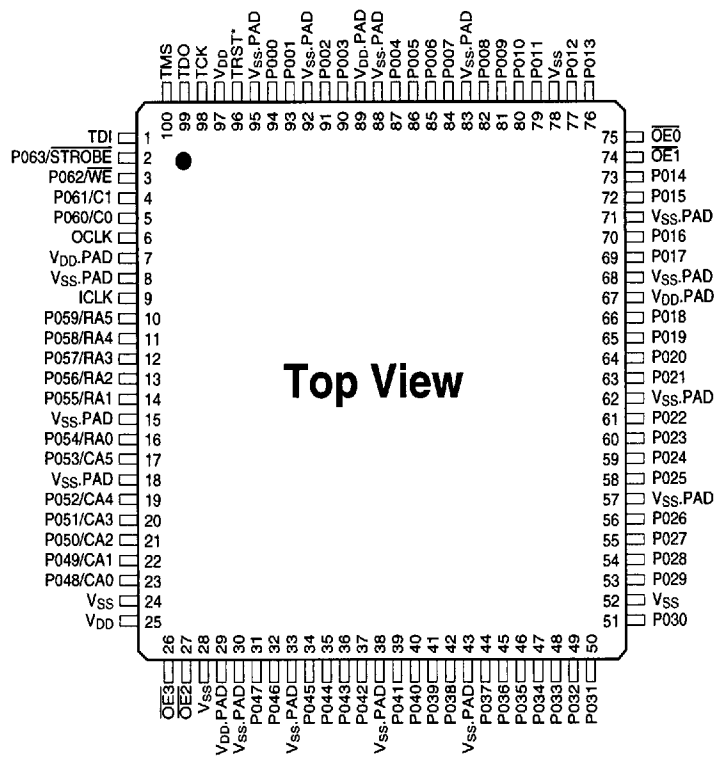
IQ64B [[MQUAD® and PQFP/100L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TDI	26	$\overline{OE3}$	51	P030	76	P013
2	P063/$\overline{STROBE}$	27	$\overline{OE2}$	52	V_{SS}	77	P012
3	P062/$\overline{WE}$	28	V_{SS}	53	P029	78	V_{SS}
4	P061/C1	29	V_{DD}.PAD	54	P028	79	P011
5	P060/C0	30	V_{SS}.PAD	55	P027	80	P010
6	OCLK	31	P047	56	P026	81	P009
7	V_{DD}.PAD	32	P046	57	V_{SS}.PAD	82	P008
8	V_{SS}.PAD	33	V_{SS}.PAD	58	P025	83	V_{SS}.PAD
9	ICLK	34	P045	59	P024	84	P007
10	P059/RA5	35	P044	60	P023	85	P006
11	P058/RA4	36	P043	61	P022	86	P005
12	P057/RA3	37	P042	62	V_{SS}.PAD	87	P004
13	P056/RA2	38	V_{SS}.PAD	63	P021	88	V_{SS}.PAD
14	P055/RA1	39	P041	64	P020	89	V_{DD}.PAD
15	V_{SS}.PAD	40	P040	65	P019	90	P003
16	P054/RA0	41	P039	66	P018	91	P002
17	P053/CA5	42	P038	67	V_{DD}.PAD	92	V_{SS}.PAD
18	V_{SS}.PAD	43	V_{SS}.PAD	68	V_{SS}.PAD	93	P001
19	P052/CA4	44	P037	69	P017	94	P000
20	P051/CA3	45	P036	70	P016	95	V_{SS}.PAD
21	P050/CA2	46	P035	71	V_{SS}.PAD	96	TRST*
22	P049/CA1	47	P034	72	P015	97	V_{DD}
23	P048/CA0	48	P033	73	P014	98	TCK
24	V_{SS}	49	P032	74	$\overline{OE1}$	99	TDO
25	V_{DD}	50	P031	75	$\overline{OE0}$	100	TMS



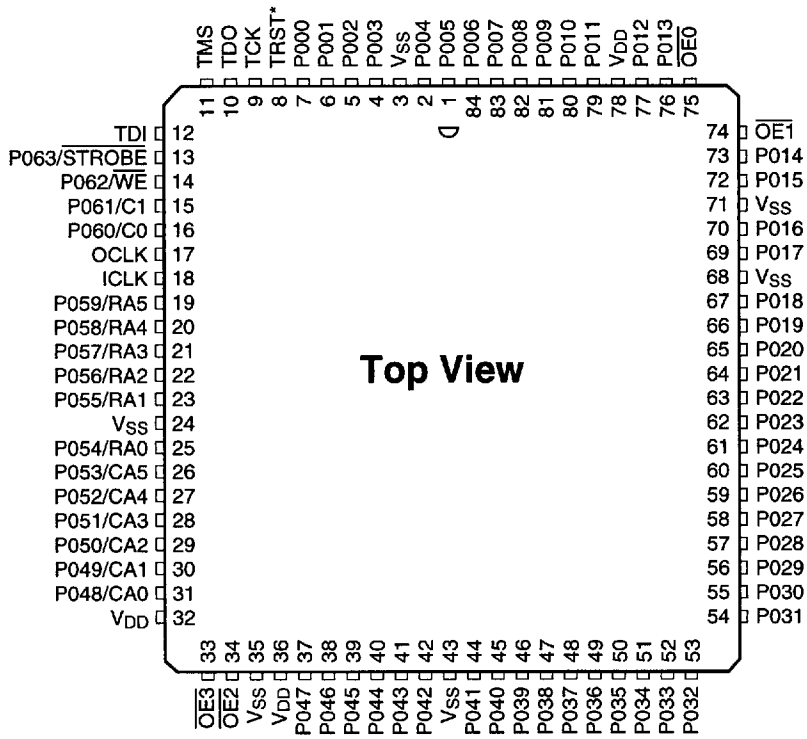
IQ64B [TQFP/100L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TDI	26	$\overline{OE3}$	51	P030	76	P013
2	P063/$\overline{STROBE}$	27	$\overline{OE2}$	52	V_{SS}	77	P012
3	P062/$\overline{WE}$	28	V_{SS}	53	P029	78	V_{SS}
4	P061/C1	29	V_{DD}.PAD	54	P028	79	P011
5	P060/C0	30	V_{SS}.PAD	55	P027	80	P010
6	OCLK	31	P047	56	P026	81	P009
7	V_{DD}.PAD	32	P046	57	V_{SS}.PAD	82	P008
8	V_{SS}.PAD	33	V_{SS}.PAD	58	P025	83	V_{SS}.PAD
9	ICLK	34	P045	59	P024	84	P007
10	P059/RA5	35	P044	60	P023	85	P006
11	P058/RA4	36	P043	61	P022	86	P005
12	P057/RA3	37	P042	62	V_{SS}.PAD	87	P004
13	P056/RA2	38	V_{SS}.PAD	63	P021	88	V_{SS}.PAD
14	P055/RA1	39	P041	64	P020	89	V_{DD}.PAD
15	V_{SS}.PAD	40	P040	65	P019	90	P003
16	P054/RA0	41	P039	66	P018	91	P002
17	P053/CA5	42	P038	67	V_{DD}.PAD	92	V_{SS}.PAD
18	V_{SS}.PAD	43	V_{SS}.PAD	68	V_{SS}.PAD	93	P001
19	P052/CA4	44	P037	69	P017	94	P000
20	P051/CA3	45	P036	70	P016	95	V_{SS}.PAD
21	P050/CA2	46	P035	71	V_{SS}.PAD	96	TRST*
22	P049/CA1	47	P034	72	P015	97	V_{DD}
23	P048/CA0	48	P033	73	P014	98	TCK
24	V_{SS}	49	P032	74	$\overline{OE1}$	99	TDO
25	V_{DD}	50	P031	75	$\overline{OE0}$	100	TMS



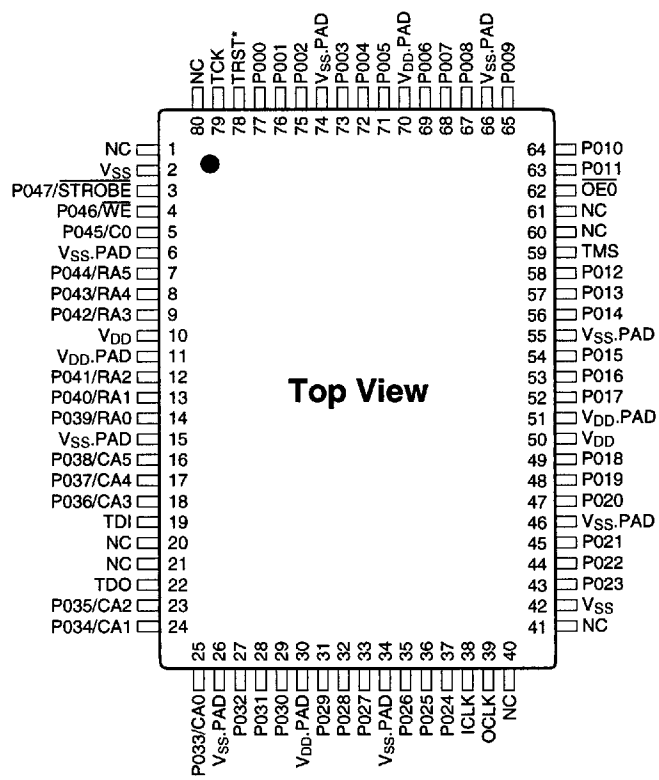
IQ64B [PLCC/84L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P005	22	P056/RA2	43	V_{SS}	64	P021
2	P004	23	P055/RA1	44	P041	65	P020
3	V_{SS}	24	V_{SS}	45	P040	66	P019
4	P003	25	P054/RA0	46	P039	67	P018
5	P002	26	P053/CA5	47	P038	68	V_{SS}
6	P001	27	P052/CA4	48	P037	69	P017
7	P000	28	P051/CA3	49	P036	70	P016
8	TRST*	29	P050/CA2	50	P035	71	V_{SS}
9	TCK	30	P049/CA1	51	P034	72	P015
10	TDO	31	P048/CA0	52	P033	73	P014
11	TMS	32	V_{DD}	53	P032	74	$\overline{OE1}$
12	TDI	33	$\overline{OE3}$	54	P031	75	$\overline{OE0}$
13	P063/$\overline{STROBE}$	34	$\overline{OE2}$	55	P030	76	P013
14	P062/$\overline{WE}$	35	V_{SS}	56	P029	77	P012
15	P061/C1	36	V_{DD}	57	P028	78	V_{DD}
16	P060/C0	37	P047	58	P027	79	P011
17	OCLK	38	P046	59	P026	80	P010
18	ICLK	39	P045	60	P025	81	P009
19	P059/RA5	40	P044	61	P024	82	P008
20	P058/RA4	41	P043	62	P023	83	P007
21	P057/RA3	42	P042	63	P022	84	P006



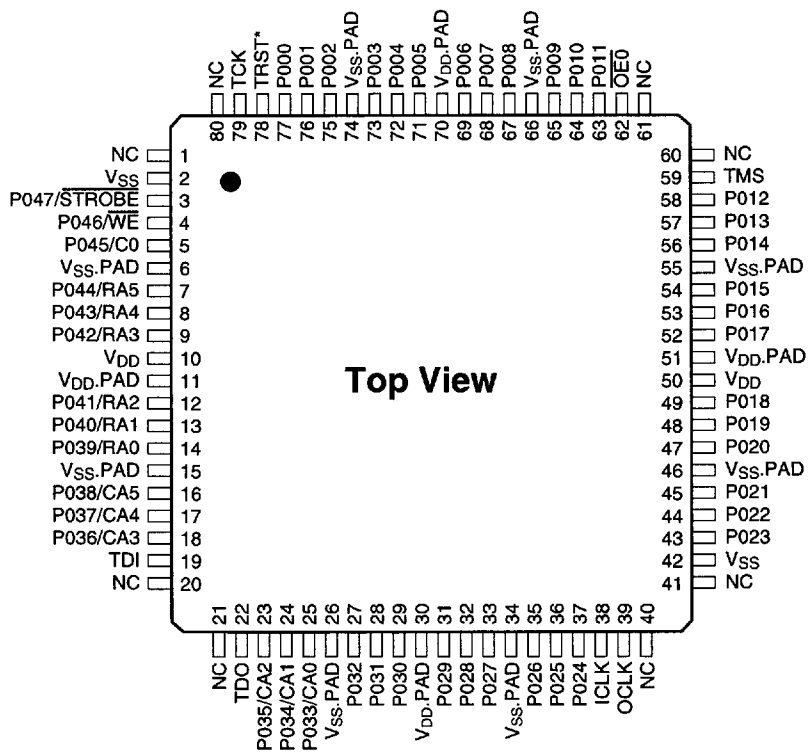
IQ48 [PQFP/80L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	NC	21	NC	41	NC	61	NC
2	V_{SS}	22	TDO	42	V_{SS}	62	$\overline{OE0}$
3	P047/$\overline{STROBE}$	23	P035/CA2	43	P023	63	P011
4	P046/$\overline{WE}$	24	P034/CA1	44	P022	64	P010
5	P045/C0	25	P033/CA0	45	P021	65	P009
6	V_{SS}.PAD	26	V_{SS}.PAD	46	V_{SS}.PAD	66	V_{SS}.PAD
7	P044/RA5	27	P032	47	P020	67	P008
8	P043/RA4	28	P031	48	P019	68	P007
9	P042/RA3	29	P030	49	P018	69	P006
10	V_{DD}	30	V_{DD}.PAD	50	V_{DD}	70	V_{DD}.PAD
11	V_{DD}.PAD	31	P029	51	V_{DD}.PAD	71	P005
12	P041/RA2	32	P028	52	P017	72	P004
13	P040/RA1	33	P027	53	P016	73	P003
14	P039/RA0	34	V_{SS}.PAD	54	P015	74	V_{SS}.PAD
15	V_{SS}.PAD	35	P026	55	V_{SS}.PAD	75	P002
16	P038/CA5	36	P025	56	P014	76	P001
17	P037/CA4	37	P024	57	P013	77	P000
18	P036/CA3	38	ICLK	58	P012	78	TRST*
19	TDI	39	OCLK	59	TMS	79	TCK
20	NC	40	NC	60	NC	80	NC



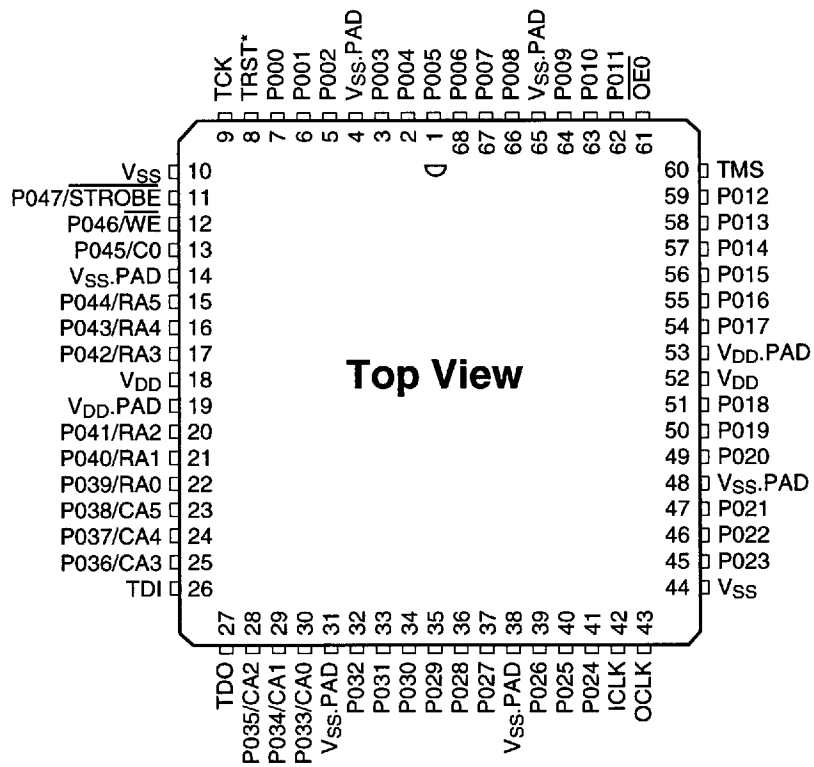
IQ48 [TQFP/80L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	NC	21	NC	41	NC	61	NC
2	V_{SS}	22	TDO	42	V_{SS}	62	$\overline{OE0}$
3	P047/$\overline{STROBE}$	23	P035/CA2	43	P023	63	P011
4	P046/$\overline{WE}$	24	P034/CA1	44	P022	64	P010
5	P045/C0	25	P033/CA0	45	P021	65	P009
6	V_{SS}.PAD	26	V_{SS}.PAD	46	V_{SS}.PAD	66	V_{SS}.PAD
7	P044/RA5	27	P032	47	P020	67	P008
8	P043/RA4	28	P031	48	P019	68	P007
9	P042/RA3	29	P030	49	P018	69	P006
10	V_{DD}	30	V_{DD}.PAD	50	V_{DD}	70	V_{DD}.PAD
11	V_{DD}.PAD	31	P029	51	V_{DD}.PAD	71	P005
12	P041/RA2	32	P028	52	P017	72	P004
13	P040/RA1	33	P027	53	P016	73	P003
14	P039/RA0	34	V_{SS}.PAD	54	P015	74	V_{SS}.PAD
15	V_{SS}.PAD	35	P026	55	V_{SS}.PAD	75	P002
16	P038/CA5	36	P025	56	P014	76	P001
17	P037/CA4	37	P024	57	P013	77	P000
18	P036/CA3	38	ICLK	58	P012	78	TRST*
19	TDI	39	OCLK	59	TMS	79	TCK
20	NC	40	NC	60	NC	80	NC



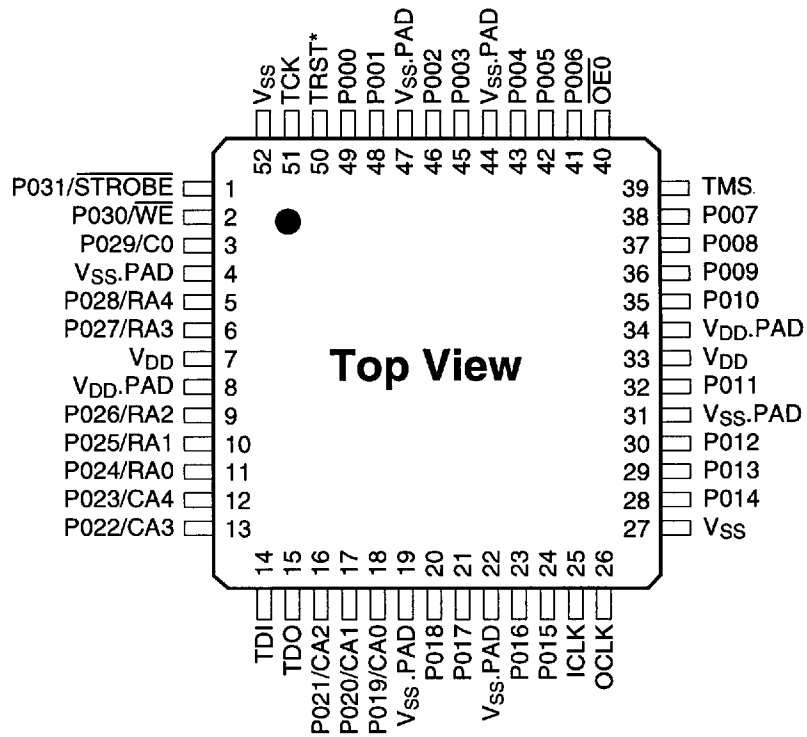
IQ48 [PLCC/68L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P005	18	V_{DD}	35	P029	52	V_{DD}
2	P004	19	V_{DD}.PAD	36	P028	53	V_{DD}.PAD
3	P003	20	P041/RA2	37	P027	54	P017
4	V_{SS}.PAD	21	P040/RA1	38	V_{SS}.PAD	55	P016
5	P002	22	P039/RA0	39	P026	56	P015
6	P001	23	P038/CA5	40	P025	57	P014
7	P000	24	P037/CA4	41	P024	58	P013
8	TRST*	25	P036/CA3	42	ICLK	59	P012
9	TCK	26	TDI	43	OCLK	60	TMS
10	V_{SS}	27	TDO	44	V_{SS}	61	$\overline{OE0}$
11	P047/$\overline{STROBE}$	28	P035/CA2	45	P023	62	P011
12	P046/$\overline{WE}$	29	P034/CA1	46	P022	63	P010
13	P045/C0	30	P033/CA0	47	P021	64	P009
14	V_{SS}.PAD	31	V_{SS}.PAD	48	V_{SS}.PAD	65	V_{SS}.PAD
15	P044/RA5	32	P032	49	P020	66	P008
16	P043/RA4	33	P031	50	P019	67	P007
17	P042/RA3	34	P030	51	P018	68	P006



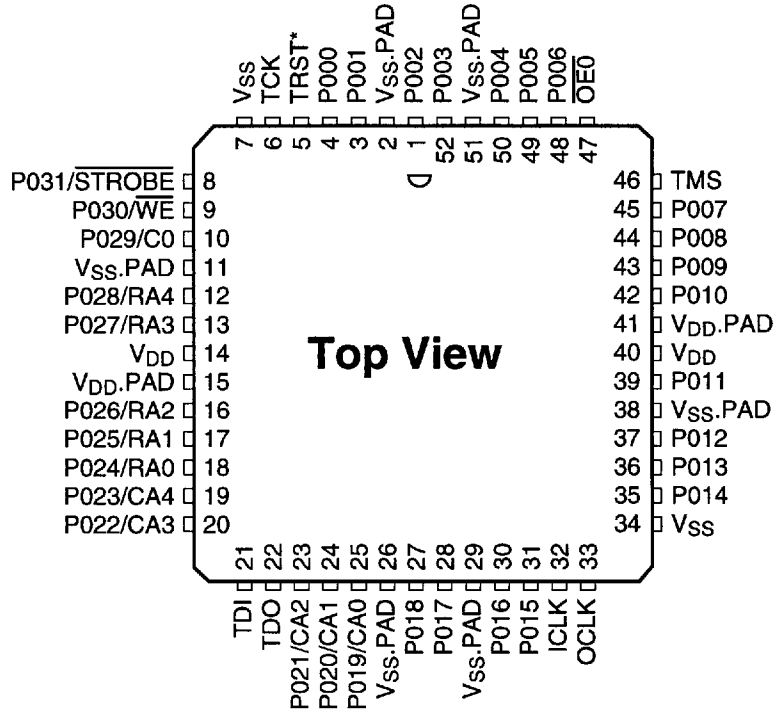
IQ32B [TQFP and PQFP/52L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P031/$\overline{\text{STROBE}}$	14	TDI	27	Vss	40	$\overline{\text{OE0}}$
2	P030/$\overline{\text{WE}}$	15	TDO	28	P014	41	P006
3	P029/C0	16	P021/CA2	29	P013	42	P005
4	V_{SS}.PAD	17	P020/CA1	30	P012	43	P004
5	P028/RA4	18	P019/CA0	31	Vss.PAD	44	Vss.PAD
6	P027/RA3	19	Vss.PAD	32	P011	45	P003
7	V_{DD}	20	P018	33	V_{DD}	46	P002
8	V_{DD}.PAD	21	P017	34	V_{DD}.PAD	47	Vss.PAD
9	P026/RA2	22	Vss.PAD	35	P010	48	P001
10	P025/RA1	23	P016	36	P009	49	P000
11	P024/RA0	24	P015	37	P008	50	TRST*
12	P023/CA4	25	ICLK	38	P007	51	TCK
13	P022/CA3	26	OCLK	39	TMS	52	Vss



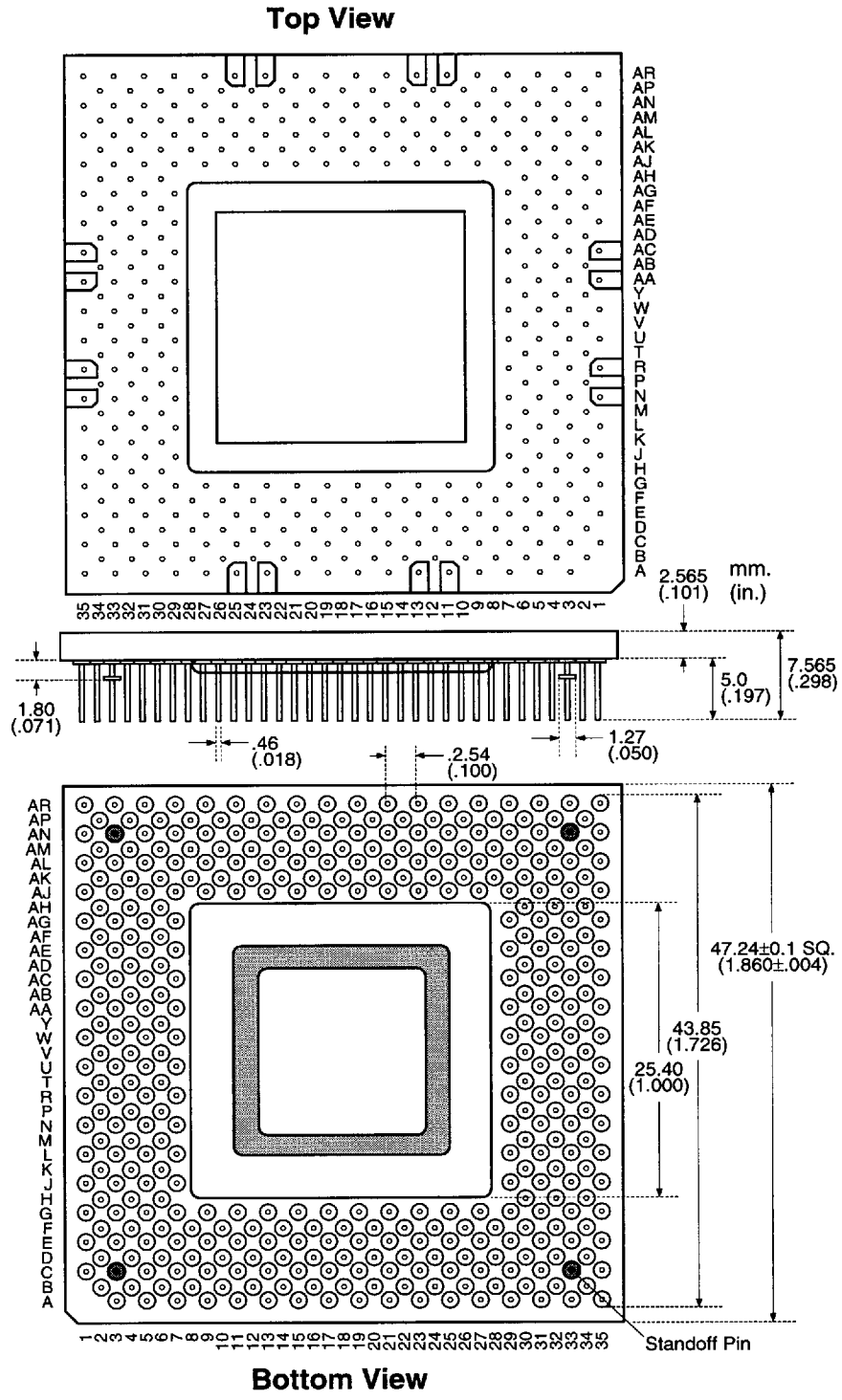
IQ32B [PLCC/52L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P002	14	V_{DD}	27	P018	40	V_{DD}
2	V_{SS}.PAD	15	V_{DD}.PAD	28	P017	41	V_{DD}.PAD
3	P001	16	P026/RA2	29	V_{SS}.PAD	42	P010
4	P000	17	P025/RA1	30	P016	43	P009
5	TRST*	18	P024/RA0	31	P015	44	P008
6	TCK	19	P023/CA4	32	ICLK	45	P007
7	V_{SS}	20	P022/CA3	33	OCLK	46	TMS
8	P031/$\overline{\text{STROBE}}$	21	TDI	34	V_{SS}	47	$\overline{\text{OE0}}$
9	P030/$\overline{\text{WE}}$	22	TDO	35	P014	48	P006
10	P029/C0	23	P021/CA2	36	P013	49	P005
11	V_{SS}.PAD	24	P020/CA1	37	P012	50	P004
12	P028/RA4	25	P019/CA0	38	V_{SS}.PAD	51	V_{SS}.PAD
13	P027/RA3	26	V_{SS}.PAD	39	P011	52	P003



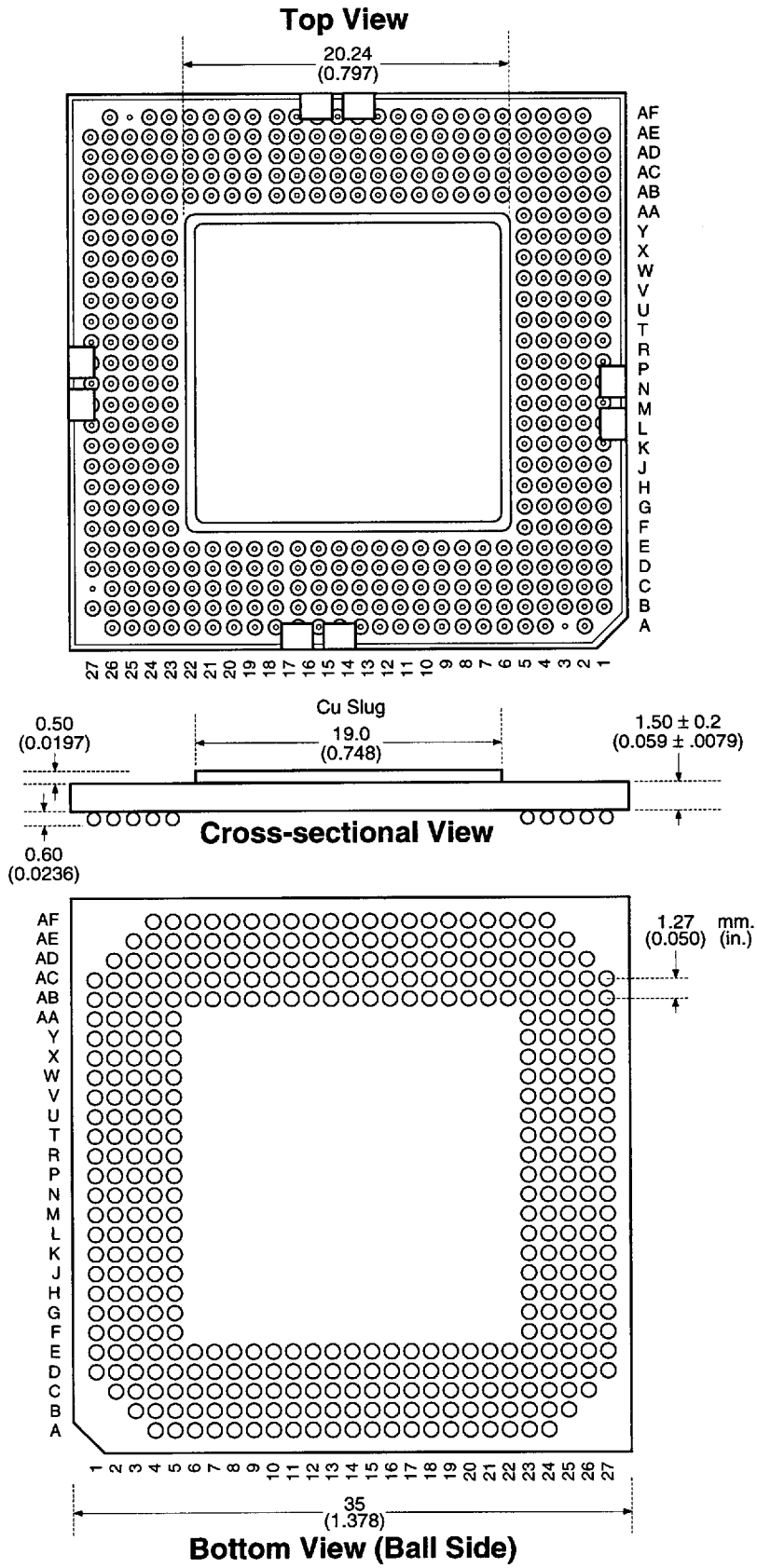
Mechanical Specification

IQ320 [PPGA/391L] Package Dimensions



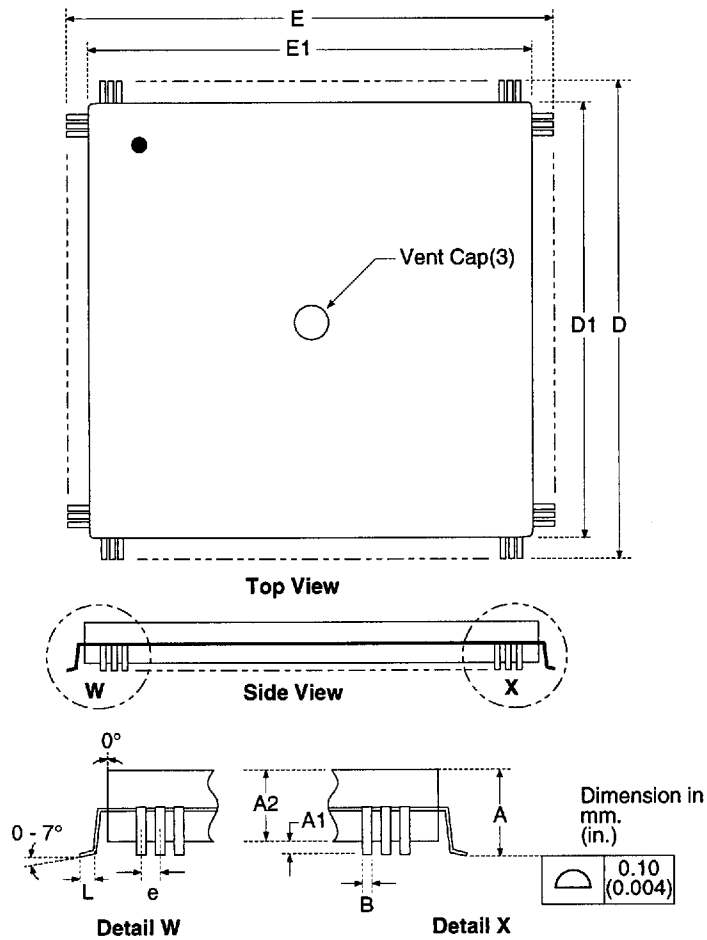
Note: Use "mm" as the controlling dimension.

IQ320 [PBGA/416L] Package Dimensions



Note: Use "mm" as the controlling dimension.

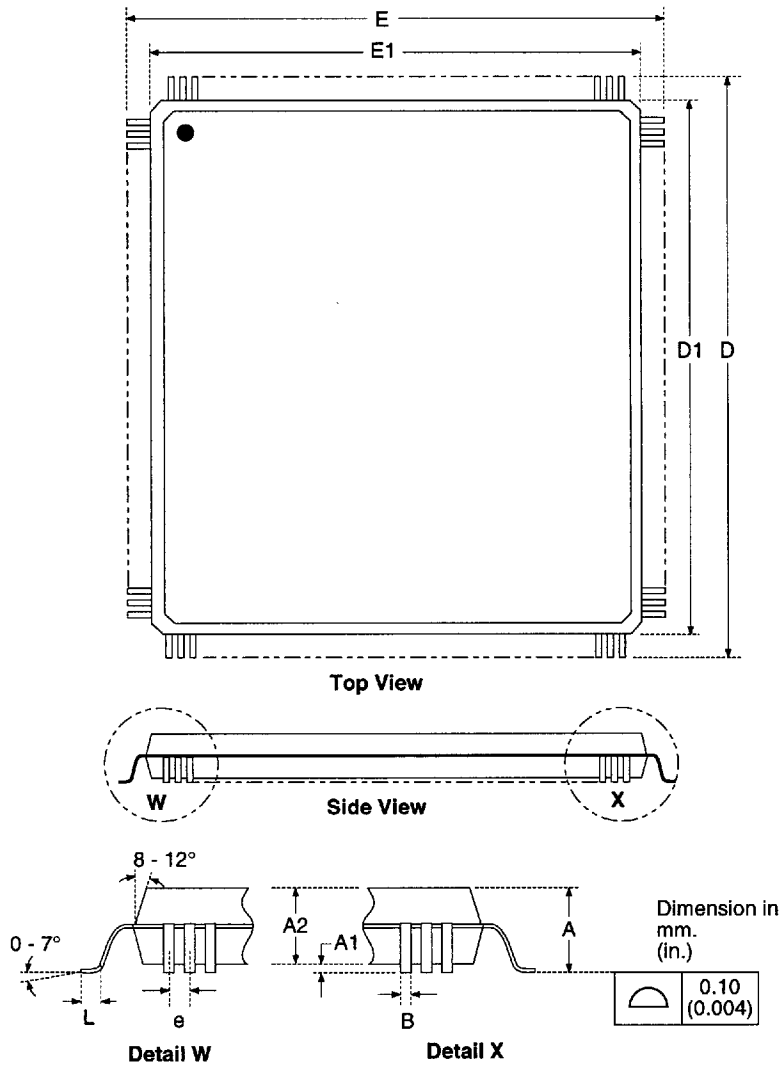
MQUAD Package Dimensions (1, 2)



Package Dimension Table		MQUAD/304L		MQUAD/208L		MQUAD/184L		MQUAD/144L		MQUAD/100L	
		inch	mm	inch	mm	inch	mm	inch	mm	inch	mm
A	max	0.172	4.38	0.156	3.96	0.156	3.96	0.152	3.96	.128	3.26
A1	min	0.010	0.25	0.014	0.35	0.014	0.35	0.014	0.35	.011	0.28
	max	0.020	0.51	0.021	0.53	0.021	0.53	0.021	0.53	.019	0.48
A2	min	0.144	3.66	0.125	3.18	0.125	3.17	0.125	3.17	.099	2.51
	max	0.154	3.92	0.135	3.43	0.135	3.43	0.135	3.43	.109	2.78
D	min	1.669	42.46	1.197	30.45	1.220	31.00	1.219	30.95	.904	22.95
	max	1.685	42.87	1.213	30.86	1.236	31.40	1.238	31.45	.923	23.45
D1	min	1.558	39.64	1.086	27.63	1.086	27.59	1.086	27.59	.779	19.74
	max	1.566	39.84	1.094	27.83	1.094	27.79	1.094	27.79	.781	19.84
E	min	1.669	42.46	1.197	30.45	1.220	31.00	1.219	30.95	.667	16.95
	max	1.685	42.87	1.213	30.86	1.236	31.40	1.238	31.45	.687	17.45
E1	min	1.558	39.64	1.086	27.63	1.086	27.59	1.086	27.59	.541	13.74
	max	1.566	39.84	1.094	27.83	1.094	27.79	1.094	27.79	.545	13.84
L	min	0.020	0.51	0.020	0.51	0.020	0.50	0.029	0.73	.029	0.73
	max	0.030	0.76	0.030	0.76	0.030	0.75	0.041	1.03	.041	1.03
B	min	0.007	0.18	0.006	0.15	0.006	0.16	0.009	0.22	.009	0.22
	max	0.011	0.28	0.011	0.28	0.011	0.27	0.014	0.35	.014	0.35
e	BSC.	0.0197	0.50	0.0197	0.50	0.0197	0.50	0.0256	0.65	.0256	0.65

Notes: (1) Use "mm" as the controlling dimension
(2) MQUAD - Metal Quad Flat Package

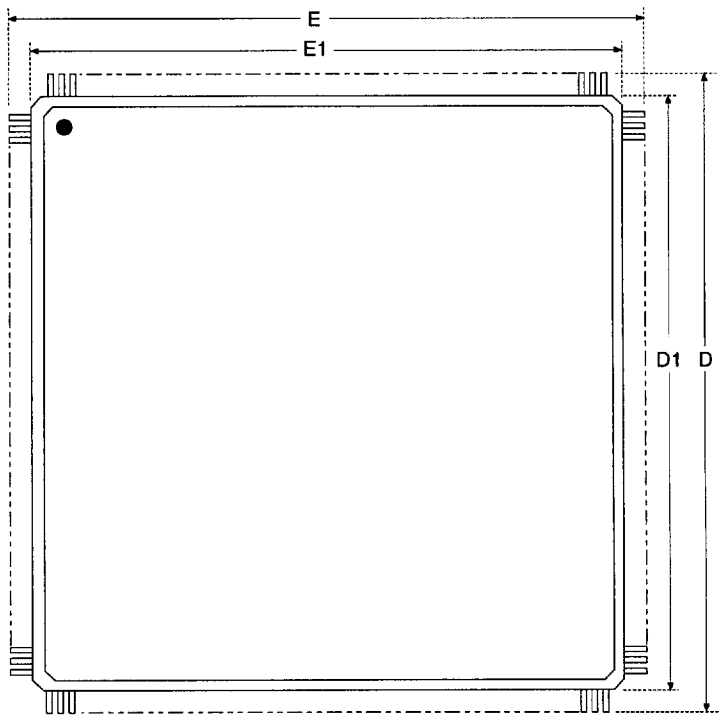
PQFP Package Dimensions (1, 2)



Package Dimension Table		PQFP/208L		PQFP/184L		PQFP/144L		PQFP/100L		PQFP/80L		PQFP/52L	
		inch	mm	inch	mm	inch	mm	inch	mm	inch	mm	inch	mm
A	max	0.157	3.99	0.157	3.99	.157	3.99	.130	3.30	.127	3.23	.096	2.45
A1	min	0.010	0.25	0.010	0.25	.010	0.25	.011	0.27	.012	0.30	.010	0.25
	max	0.017	0.43	0.017	0.43	.017	0.43	.017	0.43	.017	0.43	.015	0.38
A2	min	0.135	3.43	0.135	3.43	.135	3.43	.102	2.60	.102	2.60	.077	1.95
	max	0.140	3.56	0.140	3.56	.140	3.56	.110	2.80	.110	2.80	.081	2.07
D	min	1.195	30.40	1.219	31.01	1.219	31.01	.903	22.95	.904	22.95	.510	12.95
	max	1.215	30.91	1.238	31.49	1.238	31.49	.923	23.45	.923	23.45	.530	13.45
D1	min	1.098	27.93	1.098	27.93	1.098	27.93	.783	19.90	.783	19.90	.390	9.90
	max	1.106	28.14	1.106	28.14	1.106	28.14	.791	20.10	.791	20.10	.398	10.10
E	min	1.195	30.40	1.219	31.01	1.219	31.01	.667	16.95	.667	16.95	.510	12.95
	max	1.215	30.91	1.238	31.49	1.238	31.49	.687	17.45	.687	17.45	.530	13.45
E1	min	1.098	27.93	1.098	27.93	1.098	27.93	.547	13.90	.547	13.90	.390	9.90
	max	1.106	28.14	1.106	28.14	1.106	28.14	.555	14.10	.555	14.10	.398	10.10
L	min	0.018	0.46	0.029	0.74	.029	0.74	.023	0.60	.029	0.73	.029	0.73
	max	0.030	0.76	0.041	1.04	.041	1.04	.039	1.00	.041	1.03	.041	1.03
B	min	0.006	0.15	0.006	0.15	.009	0.23	.010	0.25	.012	0.30	.009	0.22
	max	0.011	0.28	0.011	0.28	.014	0.36	.014	0.35	.018	0.45	.014	0.35
e	BSC.	0.0197	0.50	0.0197	0.50	.0256	0.65	.0256	0.65	.0315	0.80	.0256	0.65

Notes: (1) Use "mm" as the controlling dimension
(2) PQFP- Plastic Quad Flat Package

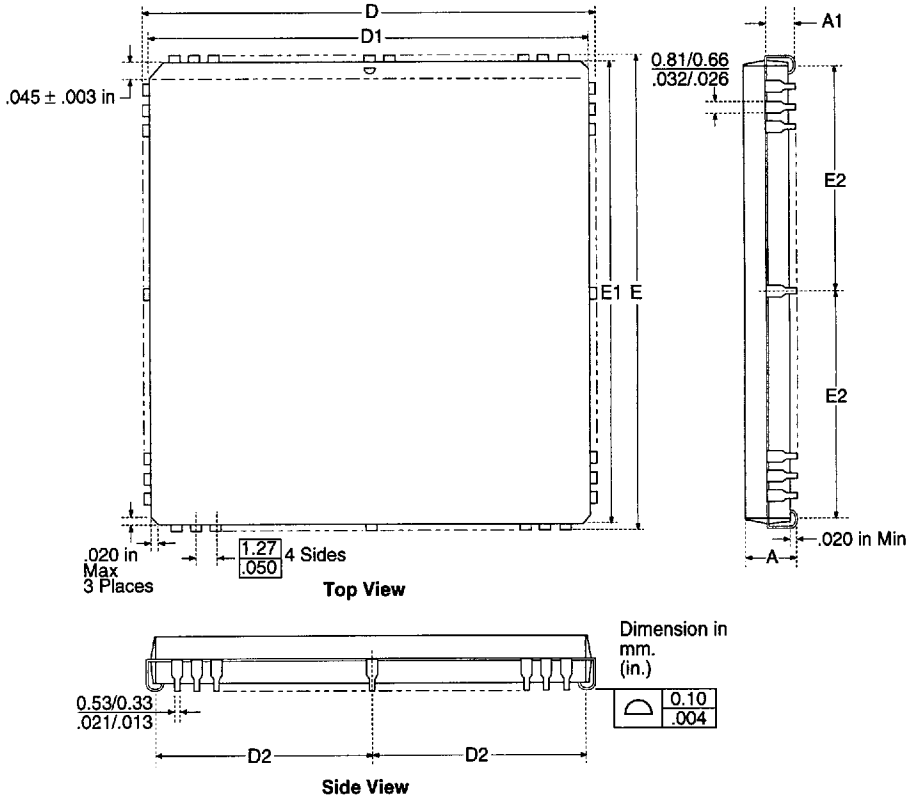
TQFP Package Dimensions (1, 2)



Package Dimension Table		TQFP/144L		TQFP/100L		TQFP/80L		TQFP/52L	
		inch	mm	inch	mm	inch	mm	inch	mm
A	max	.063	1.60	.063	1.60	.063	1.60	.063	1.60
A1	min	.002	0.05	.002	0.05	.002	0.05	.002	0.05
	max	.006	0.15	.006	0.15	.006	0.15	.006	0.15
A2	min	.053	1.35	.053	1.35	.053	1.35	.053	1.35
	max	.057	1.45	.057	1.45	.057	1.45	.057	1.45
D	min	.858	21.80	.622	15.80	.622	15.80	.465	11.80
	max	.874	22.20	.638	16.20	.638	16.20	.480	12.20
D1	min	.783	19.90	.547	13.90	.547	13.90	.390	9.90
	max	.791	20.10	.555	14.10	.555	14.10	.398	10.10
E	min	.858	21.80	.622	15.80	.622	15.80	.465	11.80
	max	.874	22.20	.638	16.20	.638	16.20	.480	12.20
E1	min	.783	19.90	.547	13.90	.547	13.90	.390	9.90
	max	.791	20.10	.555	14.10	.555	14.10	.398	10.10
L	min	.018	0.45	.012	0.30	.018	0.45	.018	0.45
	max	.030	0.75	.028	0.70	.030	0.75	.030	0.75
B	min	.007	0.17	0.007	0.17	.009	0.22	.009	0.22
	max	.011	0.2 7	0.111	0.27	.015	0.38	.015	0.38
e	BSC.	.0197	0.50	.0197	0.50	.0256	0.65	.0256	0.65

Notes: (1) Use "mm" as the controlling dimension
(2) TQFP - Thin Plastic Quad Flat Package

PLCC Package Dimensions (1, 2)



Package Dimension Table		PLCC/84L		PLCC/68L		PLCC/52L	
		inch	mm	inch	mm	inch	mm
A	max	.200	5.08	.200	5.08	.200	5.08
A1	min	.090	2.28	.090	2.28	.090	2.28
	max	.130	3.30	.130	3.30	.130	3.30
D	min	1.185	30.09	.985	25.01	.785	19.93
	max	1.195	30.35	.995	25.27	.795	20.19
D1	min	1.150	29.21	.950	24.13	.750	19.05
	max	1.158	29.41	.958	24.33	.756	19.20
D2	min	.545	13.84	.445	11.30	.345	8.76
	max	.565	14.35	.465	11.81	.365	9.27
E	min	1.185	30.09	.985	25.01	.785	19.93
	max	1.195	30.35	.995	25.27	.795	20.19
E1	min	1.150	29.21	.950	24.13	.750	19.05
	max	1.158	29.41	.958	24.33	.756	19.20
E2	min	.545	13.84	.445	11.30	.345	8.76
	max	.565	14.35	.465	11.81	.365	9.27

Notes: (1) Use inch as the controlling dimension
(2) PLCC- Plastic Leaded Chip Carrier

Component Availability and Ordering Information

The following table lists the IQ devices and the different package options, speed grades and operating temperature ranges that are currently available. Contact I-Cube Marketing for more up-to-date information on product availability.

Package	Pins	52			68	80		84	100			144			184		208		304	391	416
	Type	PQFP	TQFP	PLCC	PLCC	PQFP	TQFP	PLCC	PQFP	MQUAD	TQFP	PQFP	MQUAD	TQFP	PQFP	MQUAD	PQFP	MQUAD	MQUAD	PPGA	PBGA
	Code	PQ52	TQ52	J52	J68	PQ80	TQ80	J84	PQ100	MQ100	TQ100	PQ144	MQ144	TQ144	PQ184	MQ184	PQ208	MQ208	MQ304	PP391	PB416
IQ320	-20																			C I	C I
	-15																			C I	C I
	-12																			C	C
IQ240B	-20																		C I		
	-15																		C I		
IQ160	-20																C I	C I			
	-15																C I	C I			
	-12																C I	C I			
	-10																C	C			
IQ128B	-20														C I	C I					
	-15														C I	C I					
	-12														C I	C I					
	-10														C	C					
IQ96	-15											C I	C I	C I							
	-12											C I	C I	C I							
	-10											C I	C I	C I							
	-6											C	C	C							
IQ64B	-15							C I	C I	C I	C I										
	-12							C I	C I	C I	C I										
	-10							C I	C I	C I	C I										
	-6							C	C	C	C										
IQ48	-12				C I	C I	C I														
	-10				C I	C I	C I														
	-7				C I	C I	C I														
	-5				C	C	C														
IQ32B	-12	C I	C I	C I																	
	-10	C I	C I	C I																	
	-7	C I	C I	C I																	
	-5	C	C	C																	

C = Commercial = 0° to +70° C
I = Industrial = -40° to +85° C

Table 8: Current Component Availability